

Synopsys SystemVerilog Update

October 16th, 2003

Steve A. Smith
Sr. Marketing Director
Verification Group

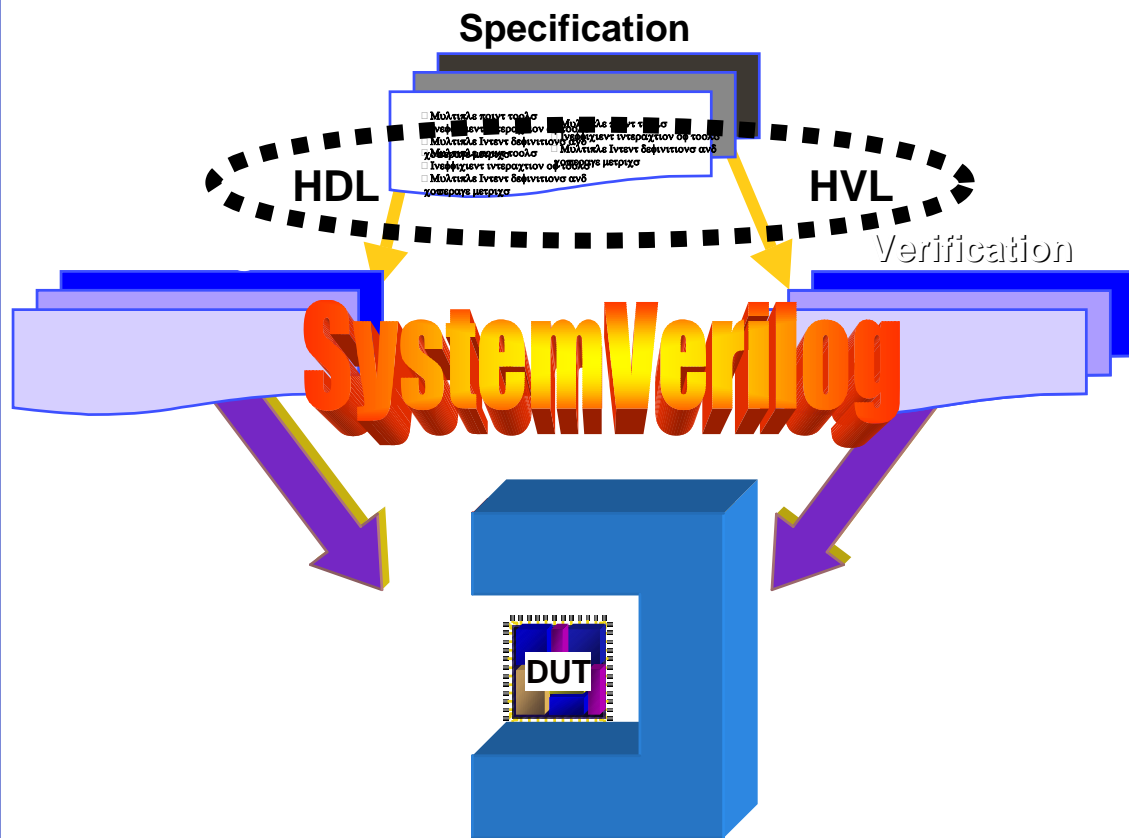


October 16, 2003

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SystemVerilog – Unifying Design and Verification

SYNOPSYS®



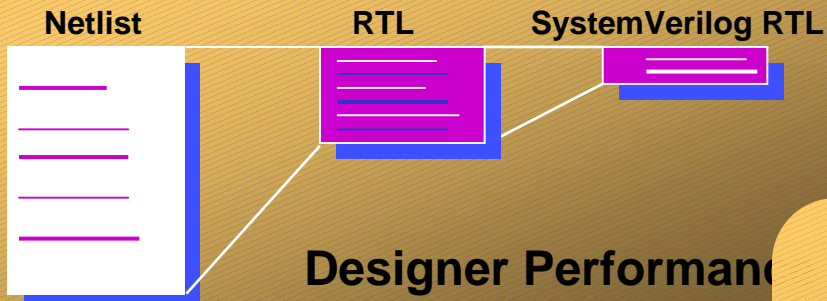
- Higher designer productivity
- Faster and smarter verification
- Evolves Verilog into a Hardware Description & Verification Language
- Growing industry momentum

Ready for Design Today!

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SystemVerilog Means Productivity

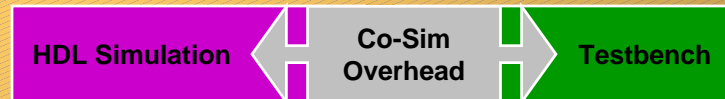
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Simulation Formal Property
Coverage Assertions Testbench

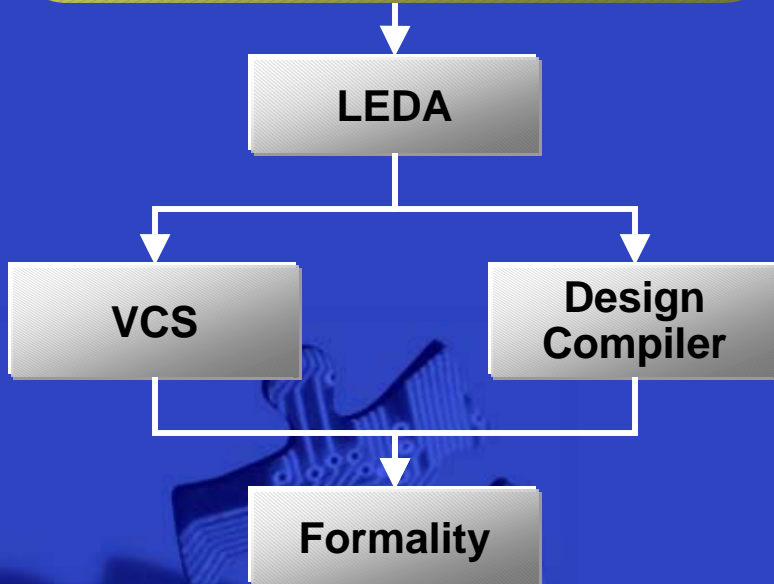
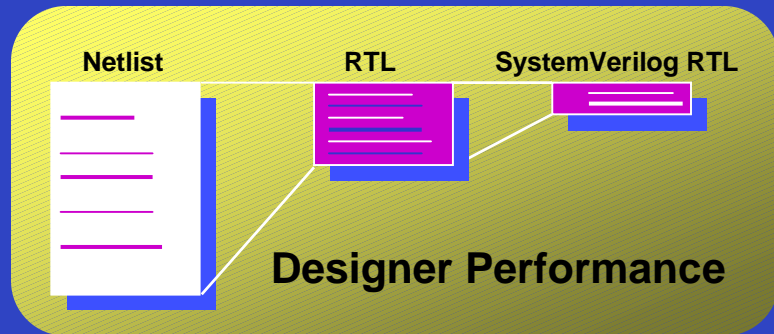
The text is arranged in two rows. The first row contains 'Simulation' and 'Formal Property'. The second row contains 'Coverage', 'Assertions', and 'Testbench'. The word 'Assertions' is highlighted in a yellow circle.

Enhanced Verification



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Synopsys SystemVerilog Tool Availability



Product	Beta Release
Design Compiler	NOW
VCS	NOW
LEDA	NOW
Formality	Q1, 2004

SystemVerilog 3.0 support now

SystemVerilog 3.1 support 1H 2004

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SystemVerilog Assertion Support in VCS

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EEdesign

Synopsys moves up SystemVerilog 3.1 support

By Richard Goering, EE Times

Sep 9, 2003 (6:30 AM)

URL: <http://www.eedesign.com/story/OEG20030909S0012>

SANTA CRUZ, Calif. — Synopsys Inc. will support SystemVerilog 3.1 assertions in its VCS simulator as early as October 2003 rather than waiting until next year as previously announced, according to Synopsys CEO Aart de Geus.

The announcement came at the Boston Synopsys User's Group (BSNUG) conference Monday (Sept. 8).



New

- VCS 7.1 Beta2: end of October 2003
- VCS/Vera will continue to support OVA

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SystemVerilog Assertions

SYNOPSYS®

- Built-in
 - no pragmas, no specialized language
 - maximum user productivity
- Easily usable by both design and verification engineers
- Reusable across both simulation & formal
 - no modifications and consistent results!
- Semantically the same as OpenVera Assertions
- Flexible implementation - inlined or separate file

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SystemVerilog Catalyst Program

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Synopsys Launches SystemVerilog Catalyst Program

More than 30 Companies Announce Support of SystemVerilog Standard

MOUNTAIN VIEW, Calif., October 6, 2003 - Synopsys, Inc. (Nasdaq: SNPS), the world leader in semiconductor design software, today announced its [SystemVerilog Catalyst Program](#). The SystemVerilog Catalyst Program is open to electronic design automation (EDA) vendors, silicon and verification intellectual property (IP) companies, and training services providers to benefit mutual customers by advancing tool interoperability and the availability of IP using the Accellera SystemVerilog standard. More than 30 companies are announcing their support for SystemVerilog at the program's launch. This broad industry support demonstrates the rapidly growing momentum for SystemVerilog adoption by leading design teams worldwide.

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SystemVerilog Catalyst Partners

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SystemVerilog NOW! Seminars

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**SystemVerilog NOW! Technical Seminars to
Be Offered across North America**

**Industry Leaders Axis Systems, Mentor Graphics,
and Synopsys to Sponsor Technical Sessions to
Immediate Benefits to Using SystemVerilog**

**> 1,000
Engineers
Registered
So Far!!**

MOUNTAIN VIEW, Calif., September 23, 2003 - Four leaders in advanced design and verification technologies-Axis Systems, Mentor Graphics (Nasdaq: MENT), Novas Software and Synopsys (Nasdaq: SNPS), with the support of HP's platform technology-are sponsoring a free SystemVerilog technical seminar and product demonstrations in four North American locations beginning October 8, 2003. Each seminar will be presented by noted Verilog design expert Cliff Cummings, president of Sunburst Design, Inc.

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Summary

SYNOPSYS®

- SystemVerilog momentum is growing
- Synopsys is committed to supporting SystemVerilog for design and verification
- VCS, Design Compiler and other tools support SystemVerilog for designers today
- Synopsys will continue to support OpenVera, OVA, Verilog, VHDL, ...



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