

Model *Sim*®

&

SystemVerilog

Mentor
Graphics®

Mentor and Standards



- **Mentor is committed to standards**
 - Representation on most committees
 - Active contribution
 - Donation of verification technology
 - Aggressively implementing standards
 - Providing chairs of Accellera, VSI Alliance and IEEE 1076



Mentor Graphics

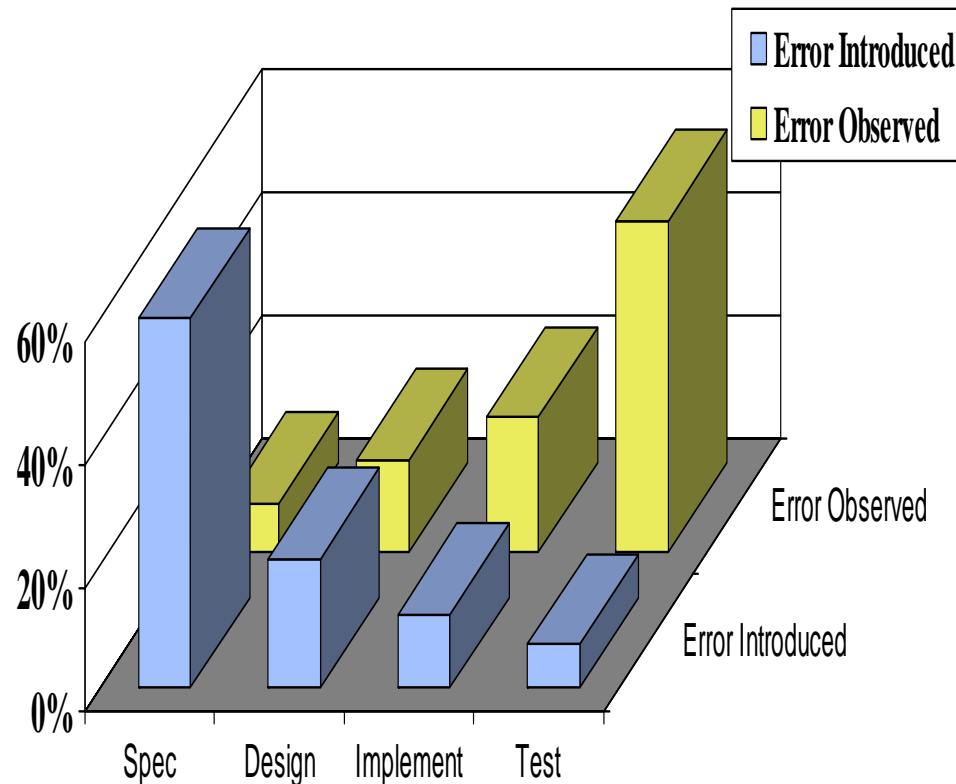
Statement on SystemVerilog



September 23, 2003

“The single largest design bottleneck electronics designers face today is design verification. Mentor Graphics has a strong history of supporting open and public standards which permit design teams to craft methodologies that utilize a broad range of verification solutions to solve this critical issue,” said Robert Hum, vice president and general manager of Mentor's Design Verification and Test division. “SystemVerilog, an emerging open and public standard, offers a comprehensive foundation to improve the overall verification process to help alleviate issues with design complexity for the Verilog user.”

Verification Trends



70% of bugs have been introduced in front end

- **Verification consumes more than 70% of the design cycle**
 - Specialization of Design and Verification teams
 - Block and system verification
 - Verifying hardware and software
 - Mixed Signal systems
 - Assertion-based verification
- **Relentless cost reduction, short market windows, increasing chip complexity**
 - More verification earlier and at higher level of abstraction
 - More first pass success
 - Productivity gains

Key Drivers in Verification



- **Performance**
 - Can my verification engines validate my designs on my schedule?
 - How do I make what I have more productive?
 - How do I leverage my knowledge and intent to improve the verification effort?

- **Finding hard bugs**
 - Cost of fixing them later is prohibitive
 - Maximize the chances of correct functionality for individual modules and the integration of these modules
 - Define and debug on multiple levels of abstraction

- **Completeness**
 - Am I done?

Design & Verification Trends



- **Specify & Verify Systems at Higher Level of Abstraction**
 - Architectural Exploration & Optimization (Hardware/Software Partitioning)
 - Validate Concepts at System Level
 - Faster Hardware & Software Cosimulation without Regard to Clocking Scheme
- **Easy Refinement to Implementation Level**
 - Refine “Executable Specification” to RTL
 - Synthesizable RTL
- **Single Environment for Design & Verification**
 - Test Bench Generation, Assertions, etc.
- **IP Development & Exchange**

ModelSim Featured at SystemVerilog Now! Seminar



- Product demo & update at SystemVerilog NOW! Seminar
- Santa Clara, CA Seminar – 10/22

Sold Out!

SystemVerilog Support
Mentor Graphics Scalable Verification

SYSTEM

Seamless C-Bridge

BLOCKS

ModelSim ADVance MS

CHIP

ModelSim ADVance MS
FormalPro
Seamless

SystemVerilog Seamless
Celaro Seamless

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ModelSim Aggressively Supports Industry Standards

Want more SystemVerilog Information?



For the latest news, sign up for ModelSim Informant at:
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