



EDA Interoperability The Good, Bad & Ugly

**Synopsys 12th EDA Interoperability Developers Forum
October 16, 2003**

Jim Hogan, Senior VP Business Development

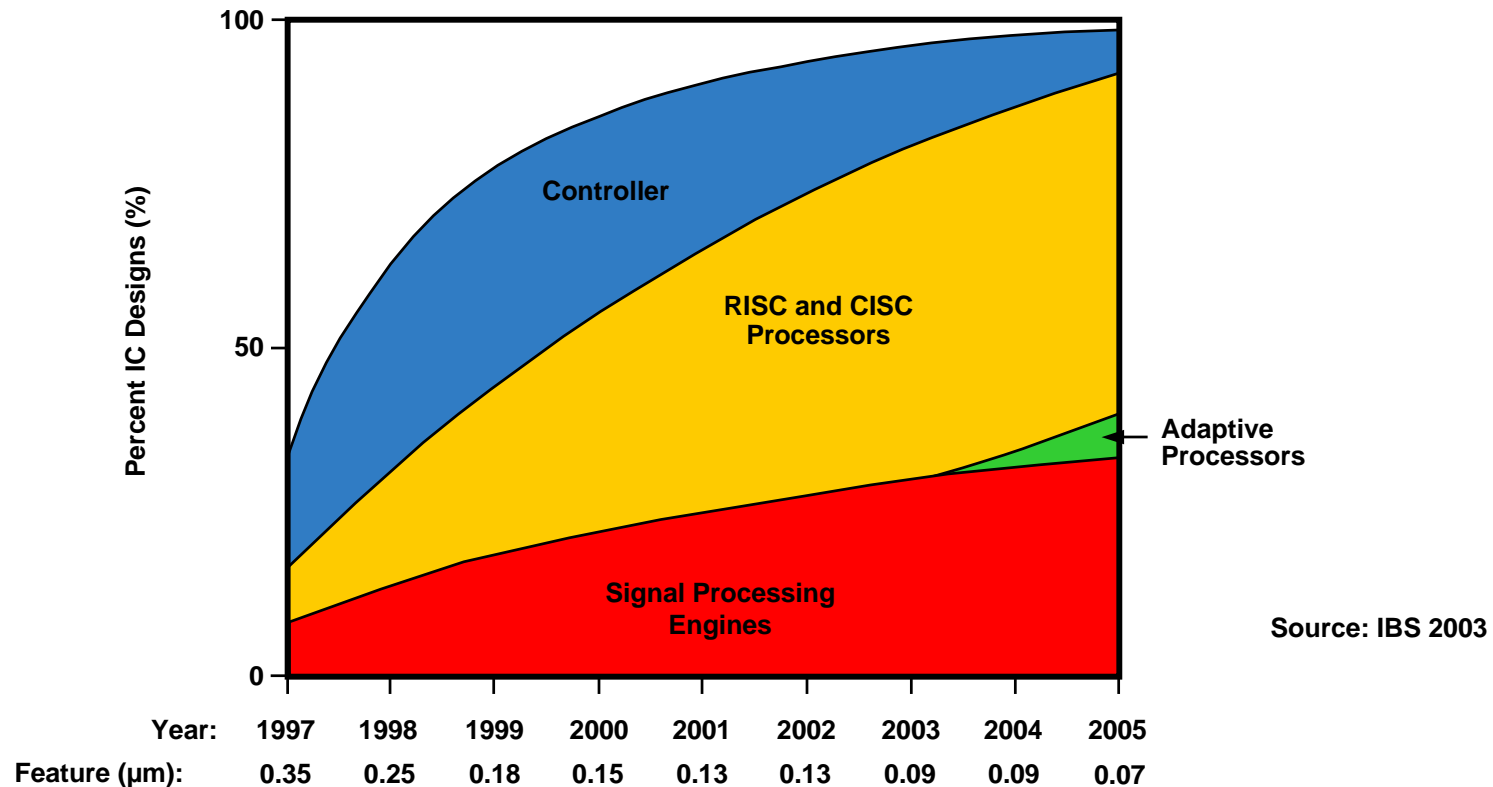
ARTISAN Components

The IP partner of choice™

Today's Discussion

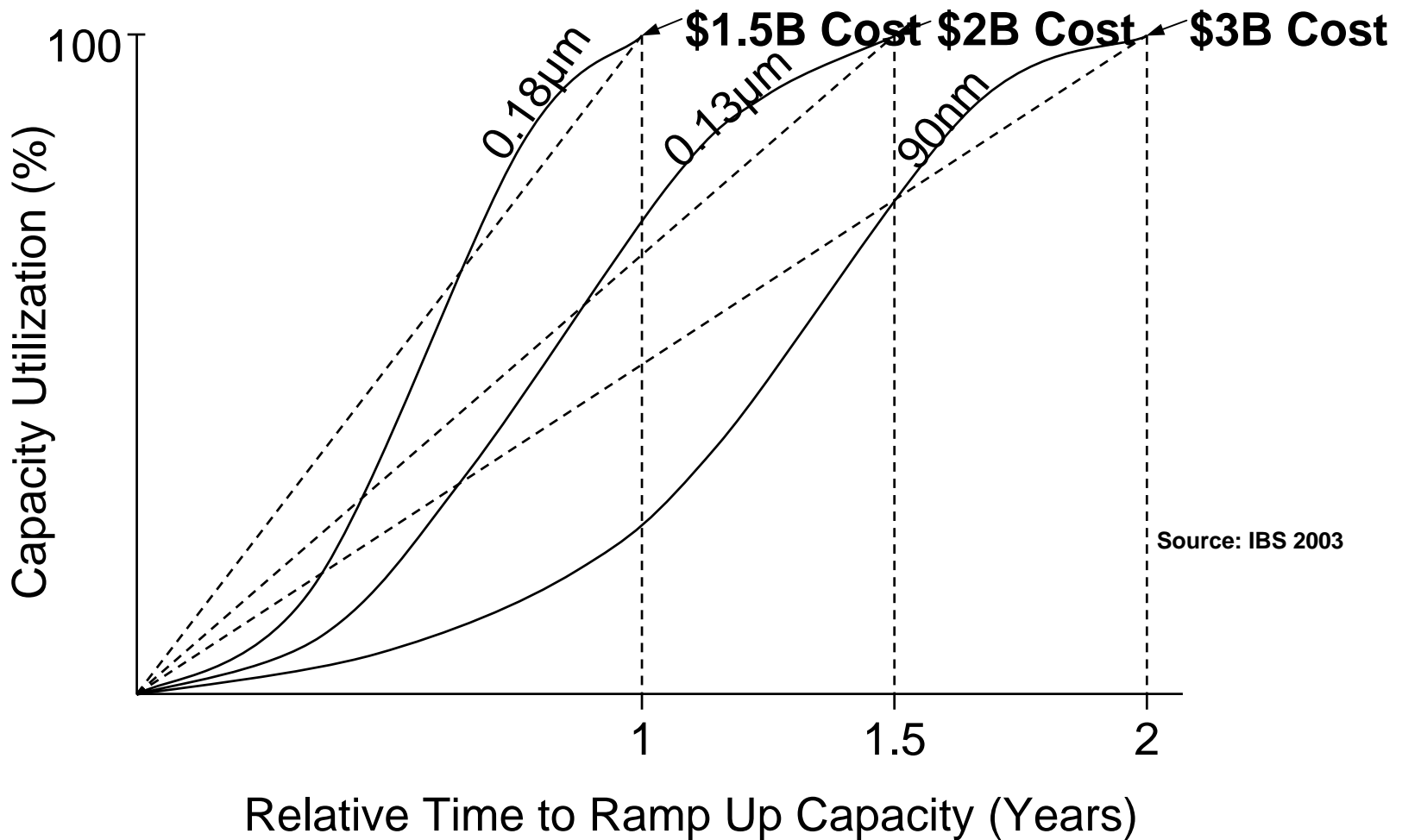
- Acknowledgements
- Market Trends
- Design Costs
- Why Standards?
- Economics of Standards
- Why Standards Fail
- Interoperability State of the Union
 - Good
 - Bad
 - Ugly
- Role of Standards in a Maturing Market
- Key Success Factors
- Summary Comments

Design Implementation Trends



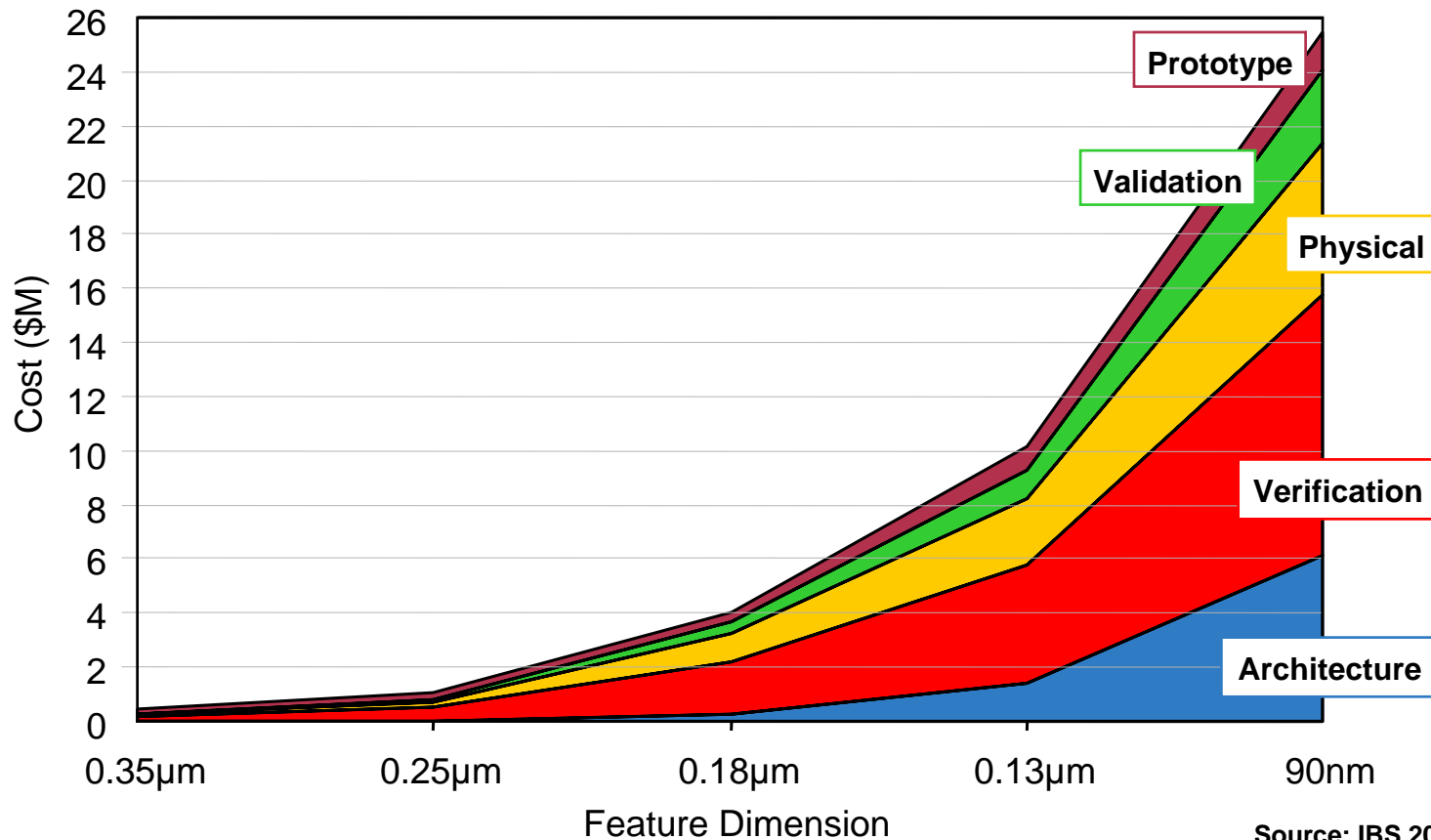
- Embedded Processors will be pervasive on SOC designs
- Hardening of the processor IP and special use blocks will be required
- Application specific design platforms, including embedded software, will be increasingly required

DFM/DFY, Designer Can Have a Positive Effect Manufacturing Variability



Source: IBS 2003

IC Design Costs (includes specification through validated prototype)

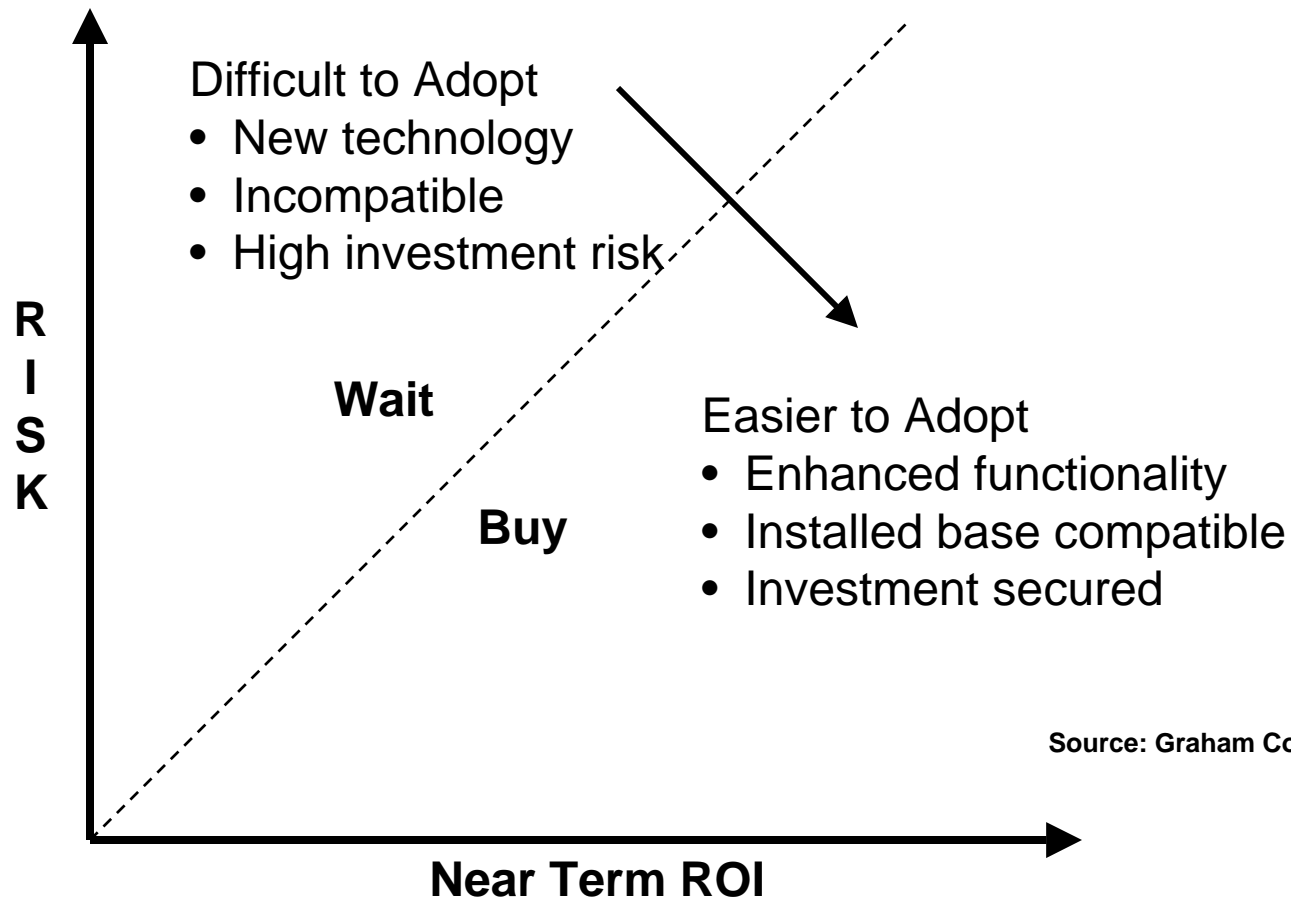


- Assuring design intent is maintained through out the entire design to manufacturing hierarchy is becoming the number one issue in silicon implementation success
- With processors so pervasive in SOC design, embedded software is increasingly an issue for design closure and verification

Why Standards?

- Good standards expand markets by:
 - Reducing the cost of vendor entry (Application S/W, Channel)
 - Spreading the risk of innovation (HTML, CDMA/GSM)
 - Seeds start-ups
 - Accelerating consumer choice (DVD, CD, MP3)
 - Opening adjacent markets (WiFi 802.11b)
 - Lowering the cost of market access
- Enhance the value of an architecture franchise
 - Examples: TI DSP, Intel PCI/PCI Express, ARM's wireless platform, et al
 - Stable roadmaps lead to long term investment
 - Overall growth through complementary products
 - Expanded reliance on the virtual supply chain or eco-system
- Directly address pent up consumer demand
 - Better functionality/cost/ease of use (RTL subset)
 - Better integration with existing devices/systems (ditto)

Economics of Standards



Why Standards Fail

- Warring tribes that miss the Big Picture of what consumers want (UNIX versus DEC/VMS)
 - Unclear customer benefit – supplier controlled the agenda
 - Companies hold on to the proprietary formats too long
- Political motivation to limit competition (DivX, IBM Microchannel)
 - Proprietary Database APIs
 - TDL/NDL netlist formats
- Customer edict without sufficient vendor input (GM Manufacturing Automation Protocol [MAP])
 - VHDL, OLA
- Difficult and significant investment to adopt - installed base incompatible
 - ALF/OLA/DCL
 - Huge installed base infrastructure investment
- Insufficient cost/benefit over existing solutions (Bluetooth)

The Good

- Major design productivity gains from abstraction
 - Verilog, re-energized the language market with significant innovation from established and start-up suppliers
 - RTL synthesizable subset
 - OK Initiative for process design kits
- Broad access to leading edge silicon through “co-opetition”
 - Library standards (.lib, LEF)
- Enabling “best of breed” methodologies and infrastructures
 - Design constraints (SDC)
 - SDF
 - DEF
 - Milkyway
 - OA

The Bad

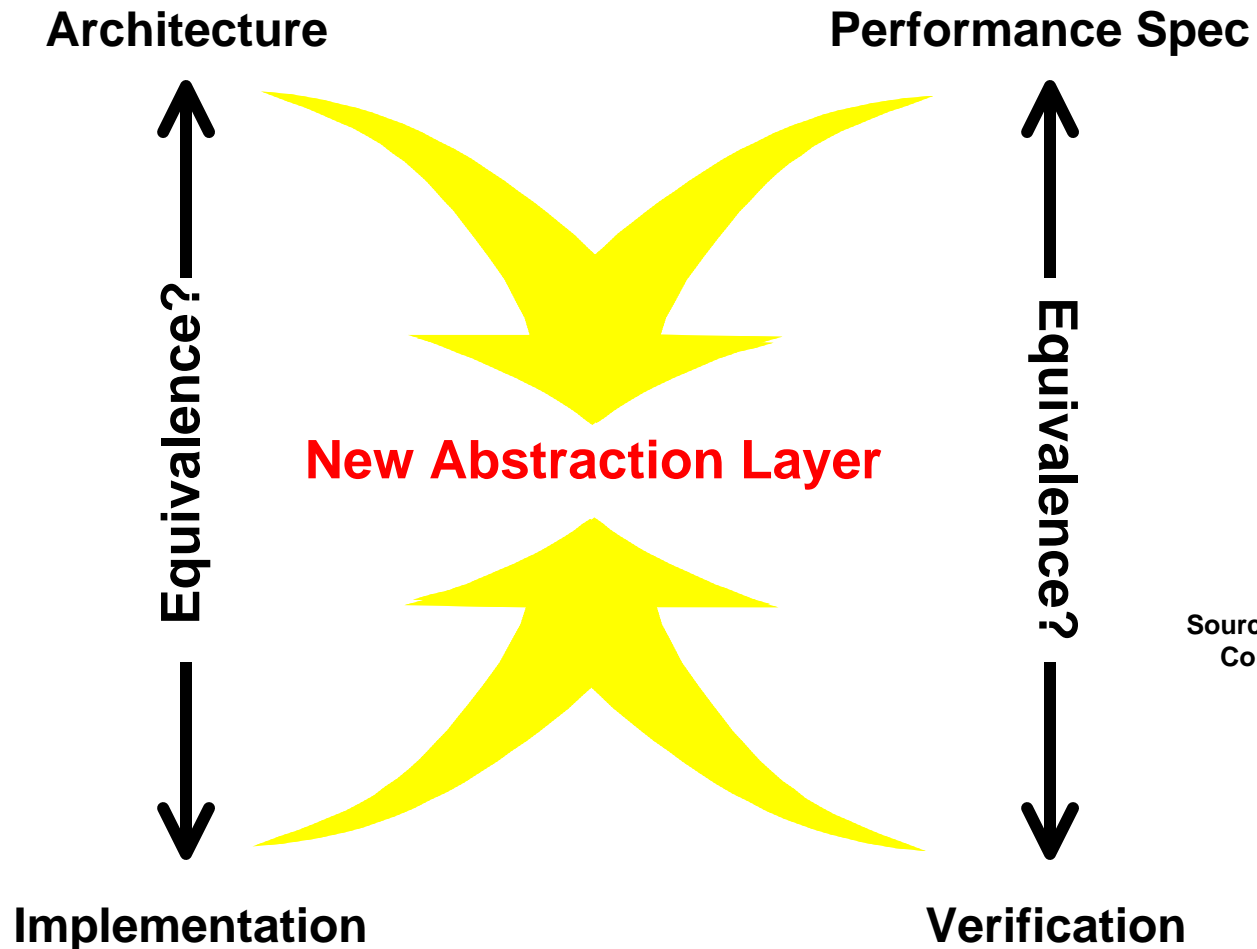
- Standards ahead of their time
 - Frameworks
 - OLA
- Solutions looking for problems
 - DCL (Design Constraint Language)
- Proprietary semantics or multiple versions
 - Perfection is the enemy of the good
 - When does opening a proprietary standard make sense (Verilog, Open Access, System C, PCI, ...)
- Abstraction without effective automation
 - Behavioral synthesis
- Quasi standards – Organic adoption
 - GDSII
 - Skill

The Ugly

- Language wars that divide scarce R&D resources with unclear benefit to users
 - Then... Verilog vs. VHDL
 - Now... System Verilog vs. IEEE1364 vs. SystemC
 - Continued politics of market share vs. market growth
- Staggering complexity of 90/65 nm processes and the attendant problem of addressing:
 - Functional Verification - more silicon more functionality
 - DFM/DFY via GDSII
- Need for a higher level of design abstraction/handoff to foster more design starts
- Optimization of multiple, simultaneous design objectives (power, timing, SI, et al)

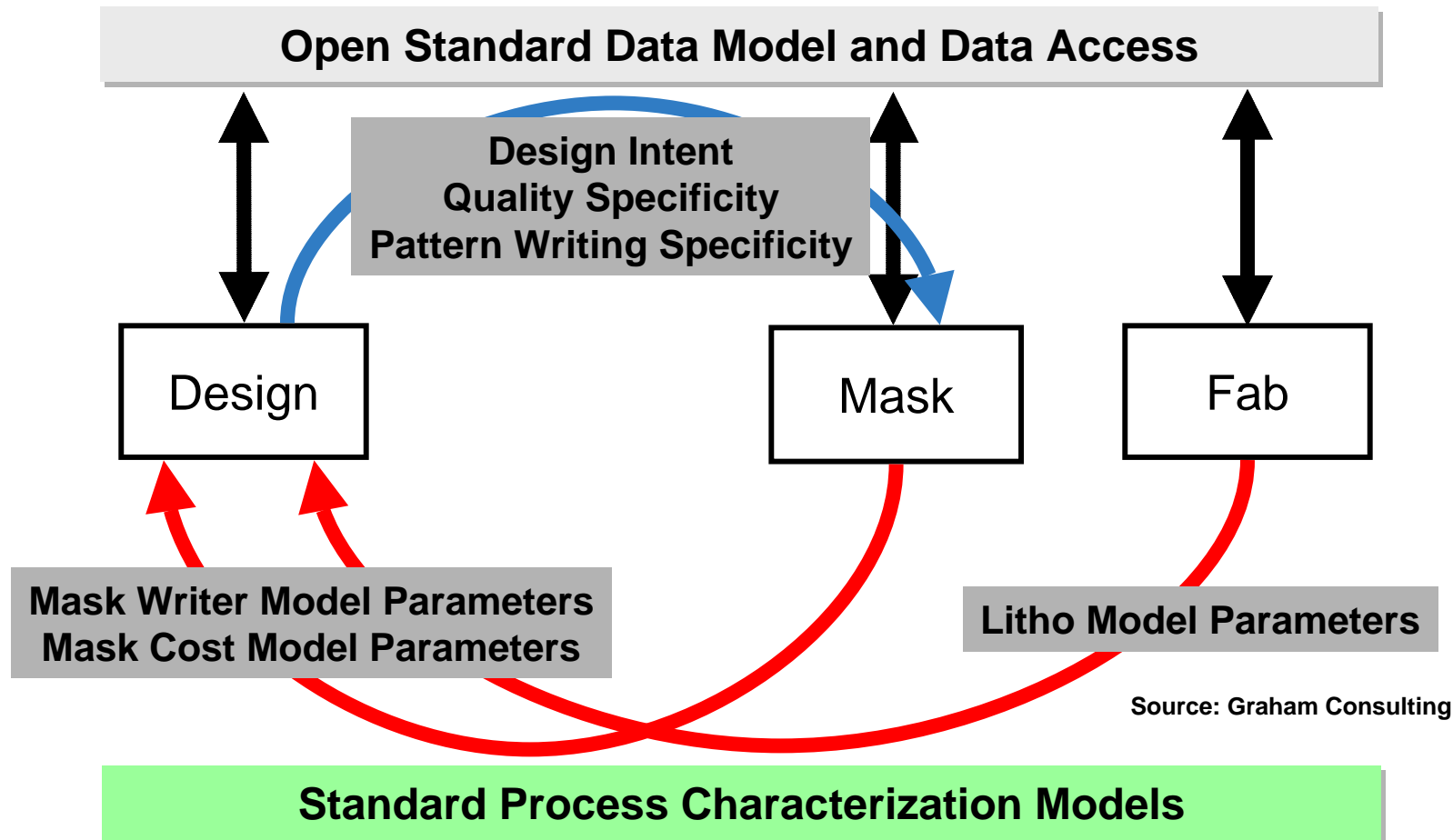
New Design Handoff Paradigm

Standard opportunities will exist at the interfaces between domains



New DFM Flow – a huge opportunity to serve the customer

Infrastructure for data sharing - design and manufacturing

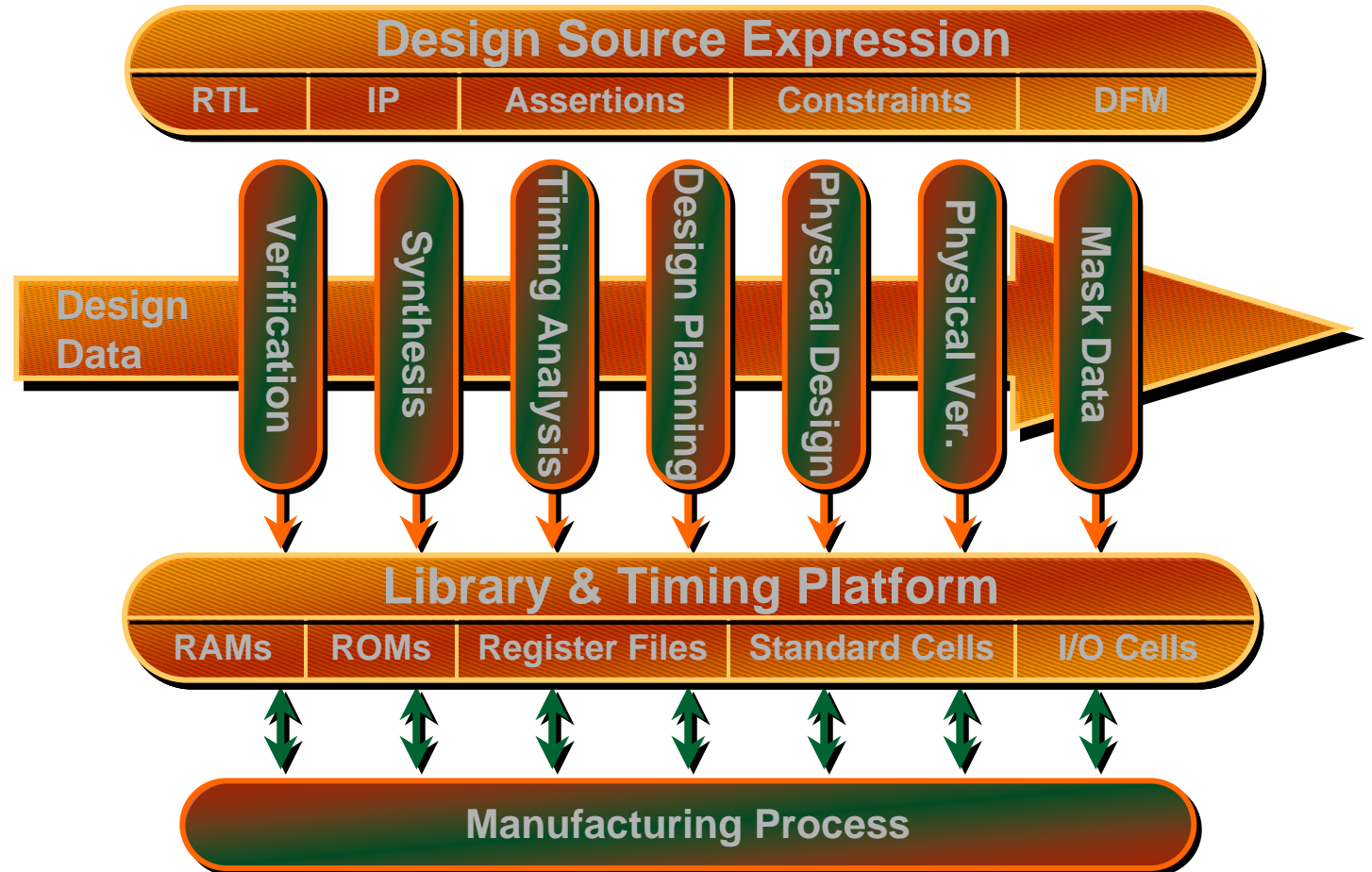


Source: Graham Consulting

The Market is Maturing...

- IC design increasingly driven by cost, efficiency and functionality over raw performance
- Cost pressures cause industry consolidation around new market aggregation layers
 - Reliance on standards to amortize the cross by member of the standards group
 - Allows for know roadmap requirements, companies innovate in the applications not the protocol
- Standards (products, architectures, interfaces, abstractions) enable economy of scale
- Economics and short product life driven by consumers have little room for religious and technical arguments
- New layers create complementary platforms for innovation and new approaches
 - Reconfigurable platforms
 - More emphasis on software
- As design complexity increases, standards play an important role of defining the articulation points

Key Articulation Layers



Source: Mark Templeton, Artisan Components

The IP partner of choice™



Collaboration Takes Many Forms

- Association – gauge trends/uncertainties and adopt policies to be implemented individually
 - SIA, FSA, SEMI
- Committee – development of a shared technical work through volunteer resources
 - MPEG, Accellera, IEEE, VSIA
- Consortium – engage in pre-competitive technology development funded by members
 - SEMATECH, SRC, Si2, STARC
- Benevolent dictatorship – market share leader/guru
 - Synopsys, TSMC, Artisan
 - Linus Torvalds
 - JAVA/SUN

Collaborative Success Factors

- Shared vision and/or mutual pain
- Clearly stated business objective and strategy
- Map 70-80% market share in area of common interest
- Define what an effective consensus means among competitors (e.g., does mutual respect/trust exist?)
- Establish balanced participation/decision making process
- Reducing risk and building trust lead to adoption

In Summary...

- The EDA industry is grappling with simultaneous technical challenges
 - **Complexity** - Improving design productivity
 - **Physics** - Inventing solutions to multiple, non-convergent optimization problems
 - **Verification** – Solving the equivalence problem
 - **Manufacturing** – DFM/DYM sensitivity throughout
- The market has matured – the EDA standards process must also rise to a new level
- Market leaders at each articulation layer should lead and cooperate to make complex design more available and attractive