

Axis Systems, Inc.

Synopsys EDA Interoperability



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CoFounder

October 2003

Outline

- Axis Overview
- System Verification Flow
- Synopsys & Axis Integration
- SystemVerilog Acceleration & Emulation
- Summary



Axis Business Focus

Solve verification productivity crisis

Deliver software and hardware verification solutions

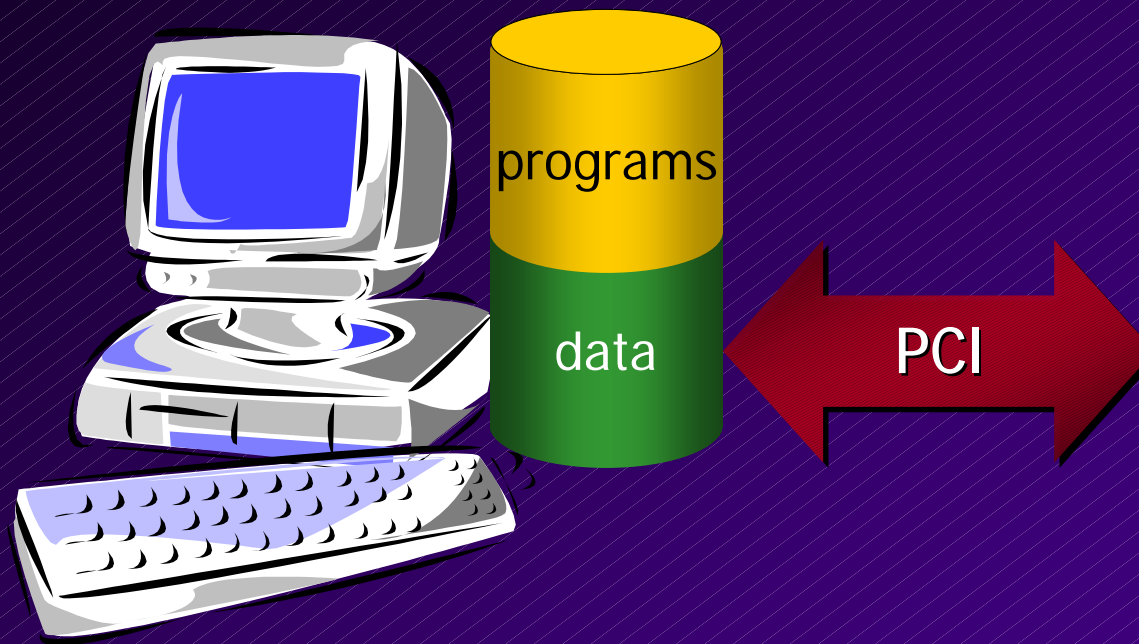
Target system and system-on-a-chip designers

Leverage breakthrough innovation of ReConfigurable Computing technology

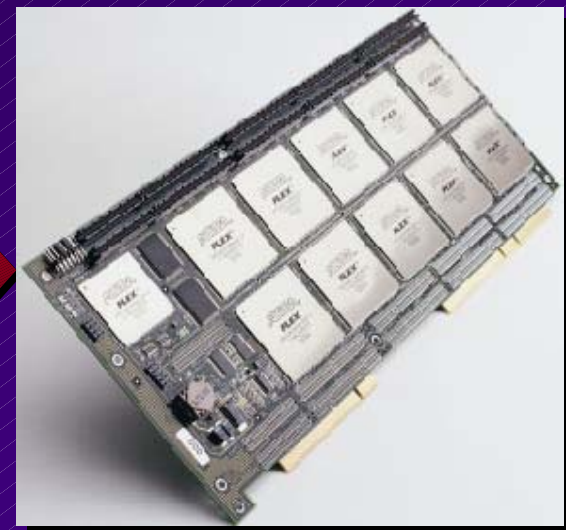


Axis Breakthrough Technology

ReConfigurable Computing (RCC) for High Performance Verification Platform



Patented RCC



Design Team Emulation (DTE)

Methodology

Methodology

- Multiple Levels of Abstraction
- Single Kernel Database
- Adv Behavioral Debugging
- Small Form Factor
- HW/SW Co-Verification

Benefits

- IP Model Reuse and Flexibility
- Fastest Bring Up - Time to Value
- Easy to Use
- Multi-team Access
- Fast and Efficient Debugging



ReConfigurable Computing (RCC)

- Design

- RTL

```

Always @(posedge clk)
begin
  rw_bus = istate;
  if (bus_active)
  .....
  .....
  
```

- Gate

```

Inv inv1 (b, a);
and and2(c, b, a);
dffp mydff(q, d, clk);
  
```

- Behavioral

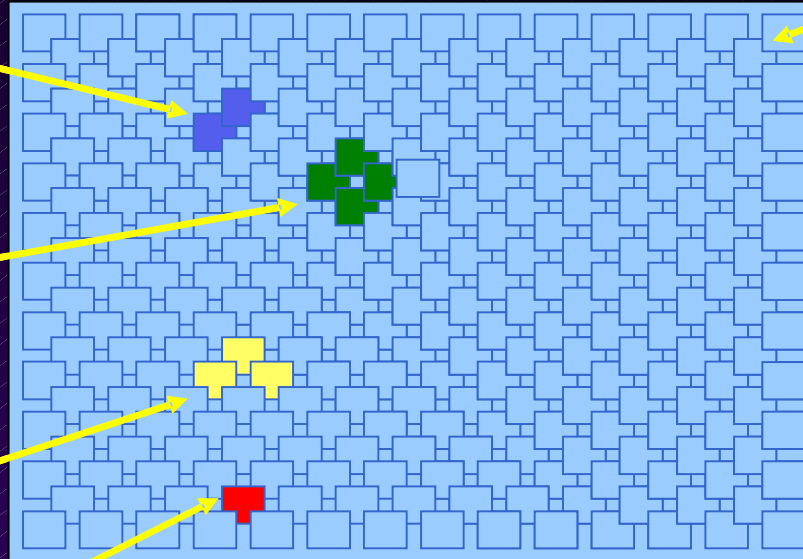
```

Initial
begin
  $monitor(...);
  $my_pli(...);
  
```

- Assertion

```

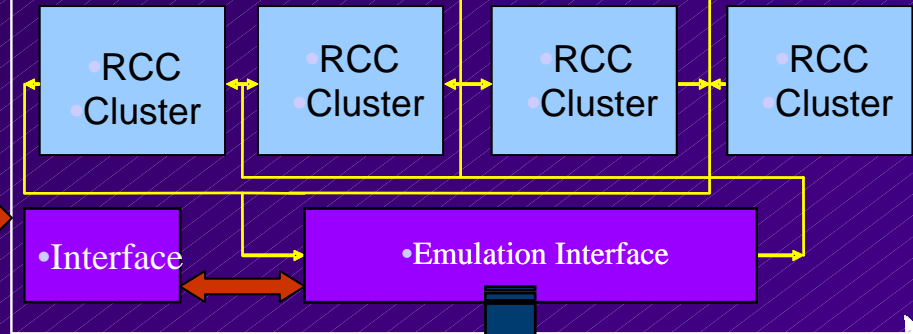
assert
(irq == 1'b0)
  
```



- Millions of
- Reconfigurable
- Computing
- Elements

- Dynamic
- Event
- Signaling

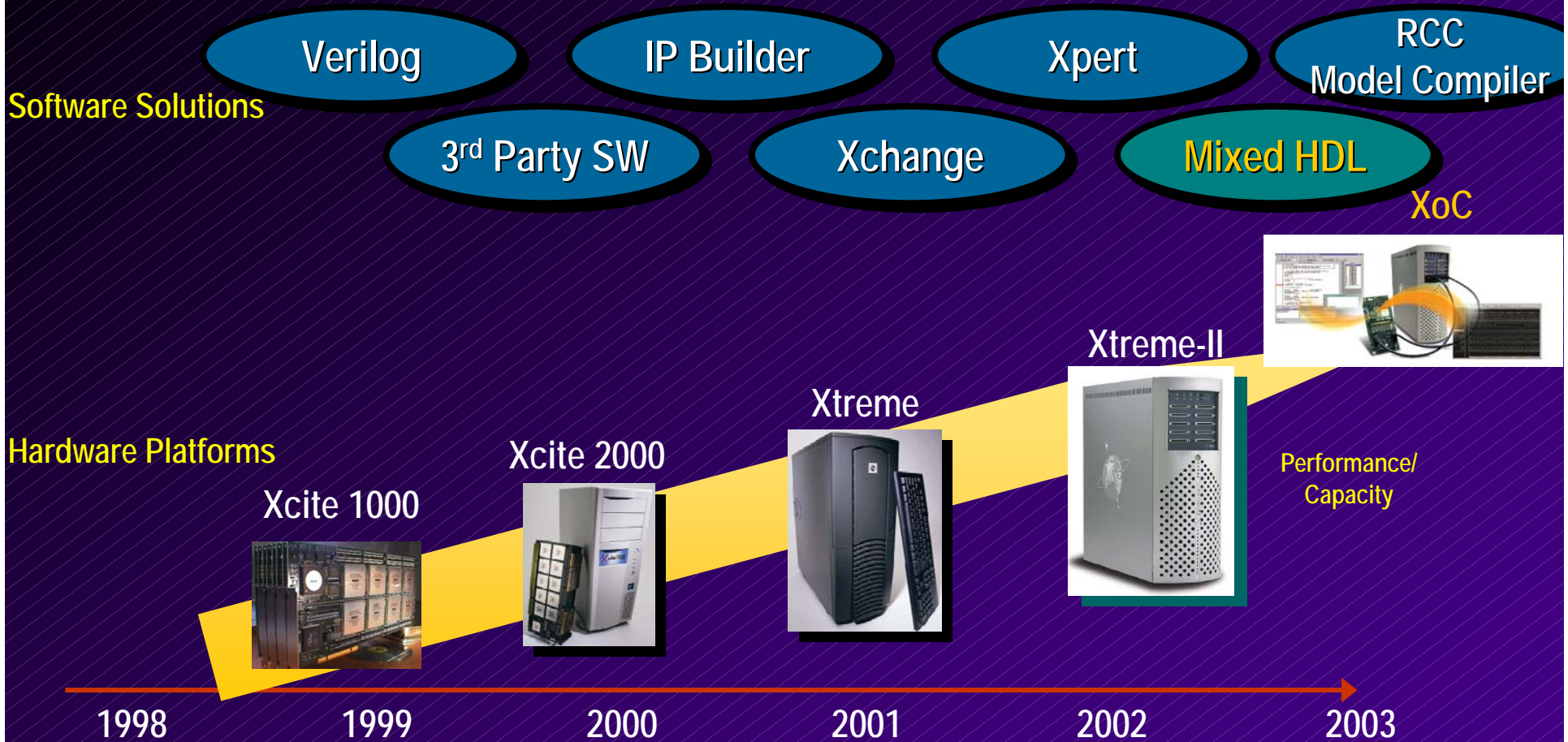
• Sun Host Workstation



Design Team Emulation



Axis Product Overview

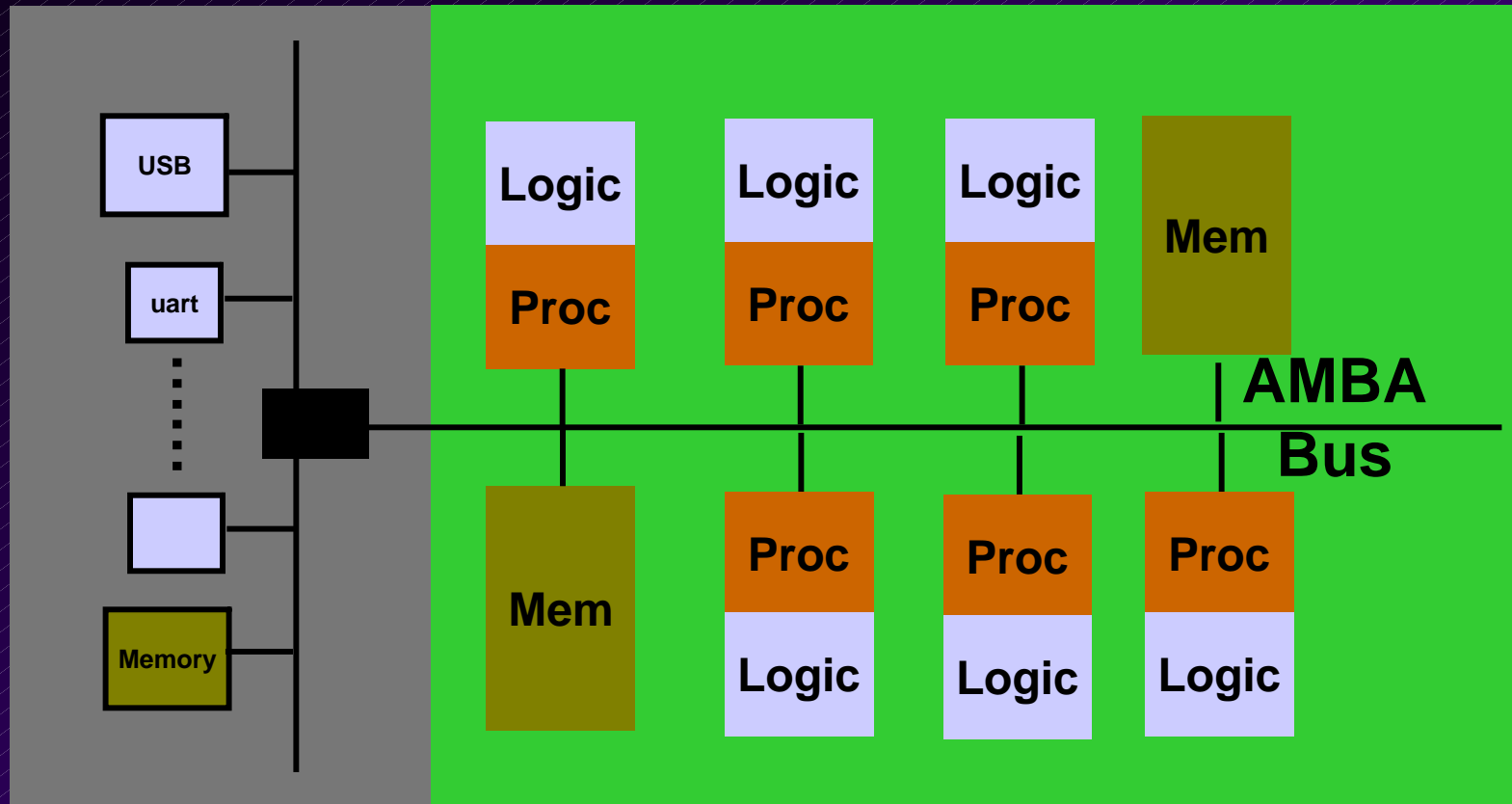


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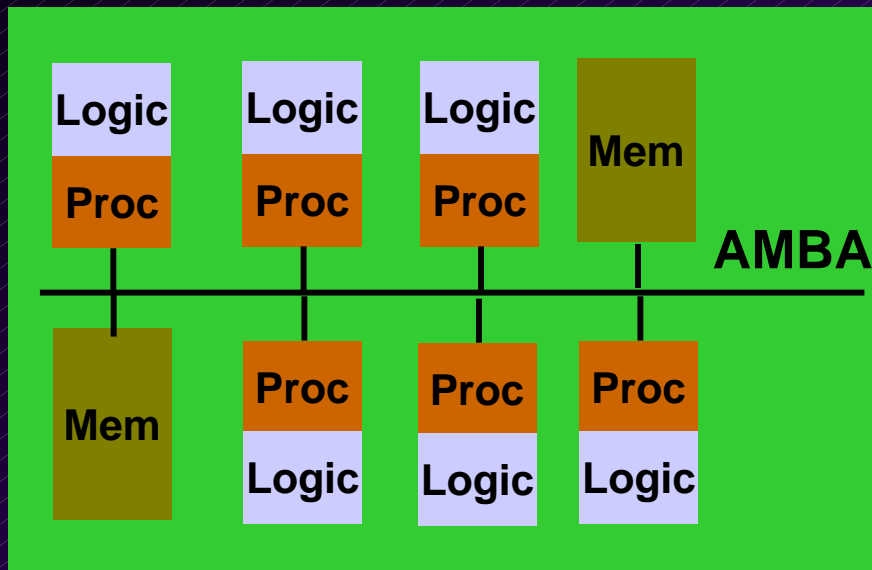
Typical SoC Architecture



Processor is standard; all logic is custom



Main Chip Functionality

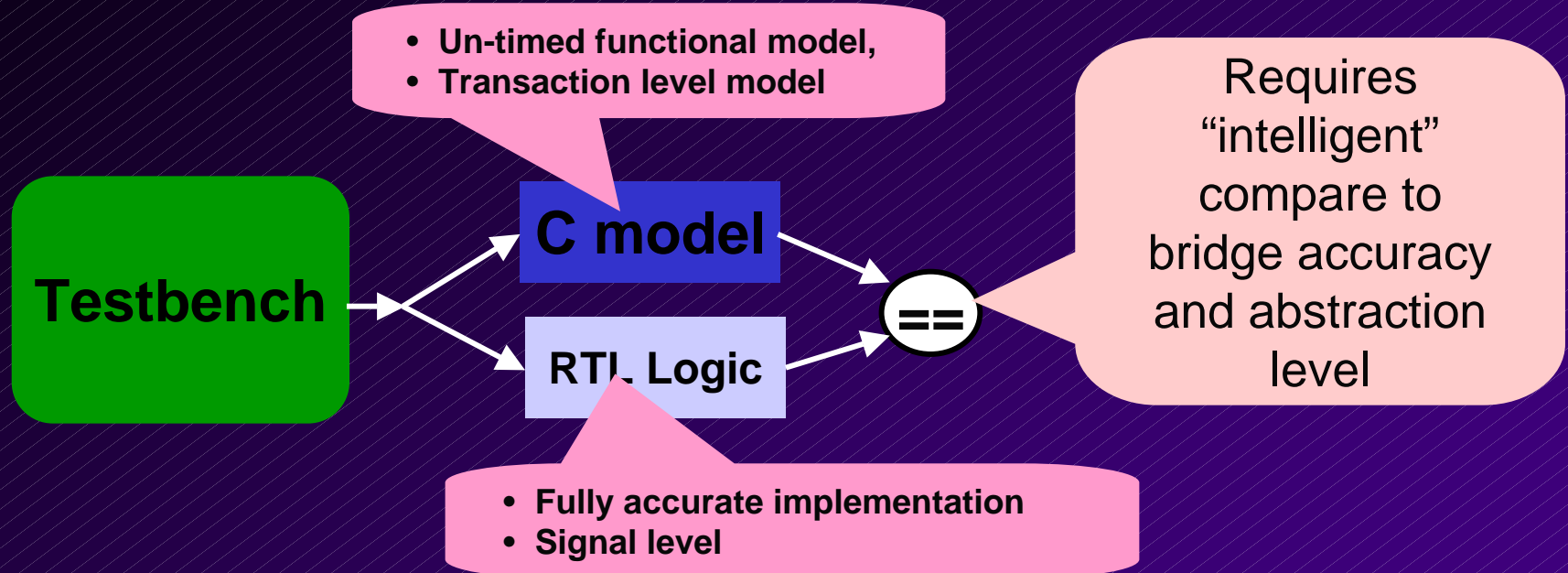


- Dedicated architecture to implement main functionality/ algorithms
 - Processor/logic (with local memory) modules
 - Shared Memory
 - Software

1. Individual module level simulation/verification
2. Full subsystem verification is always HW + embedded SW
3. Full chip (including peripherals) performed on Engineering sample



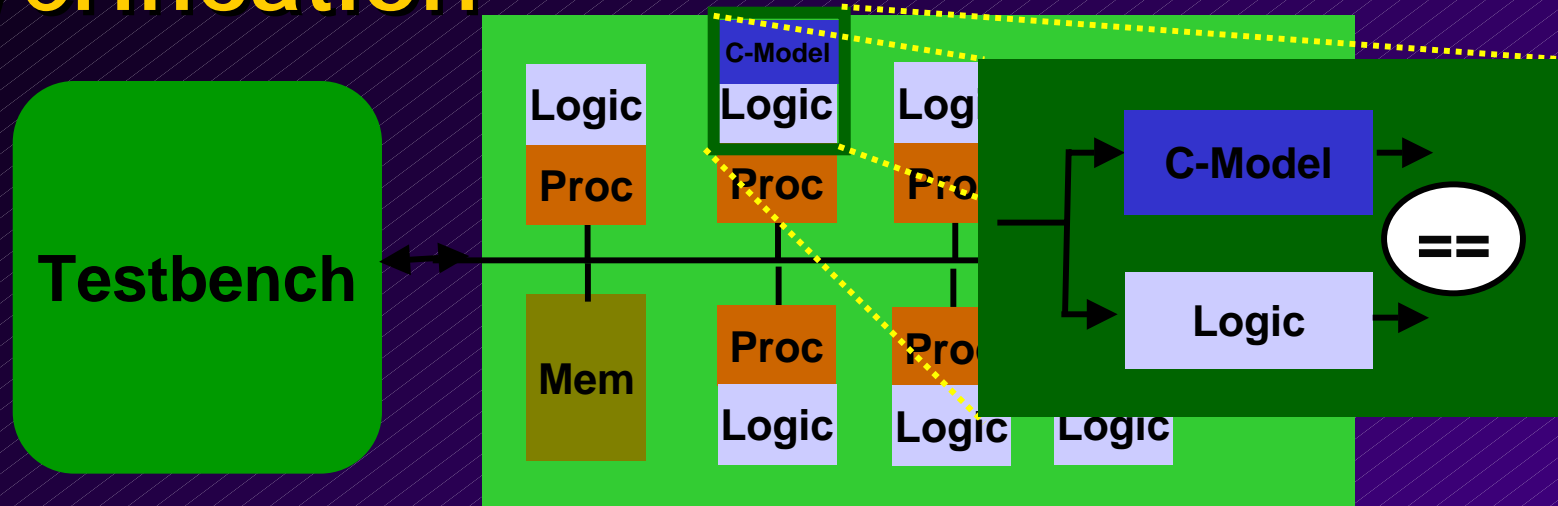
Module level verification



- Concurrent development of C-model and RTL
- C-model is mainly un-timed functional
- Both models driven from same testbench
- Reference model based verification requires C/SystemC and RTL (Verilog) co-simulation



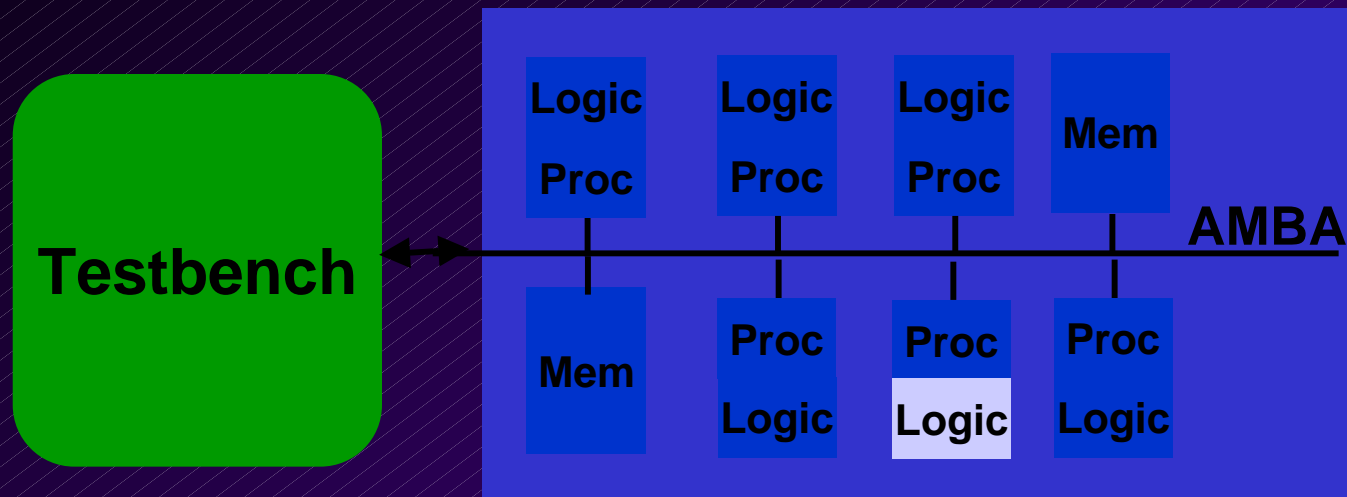
Sub-System Hardware Verification



- Reference model embedded in overall RTL architecture
- Verification with SW simulation and Axis acceleration
- Need to run embedded Software on simulated Hardware
- Testbench drives AMBA bus or other key interfaces of sub-system



Software development platform



- Software dev. Platform – Axis Emulation (1000x over RTL)
- Sometimes RTL model(s) embedded in overall System architecture
- Need to use same testbench



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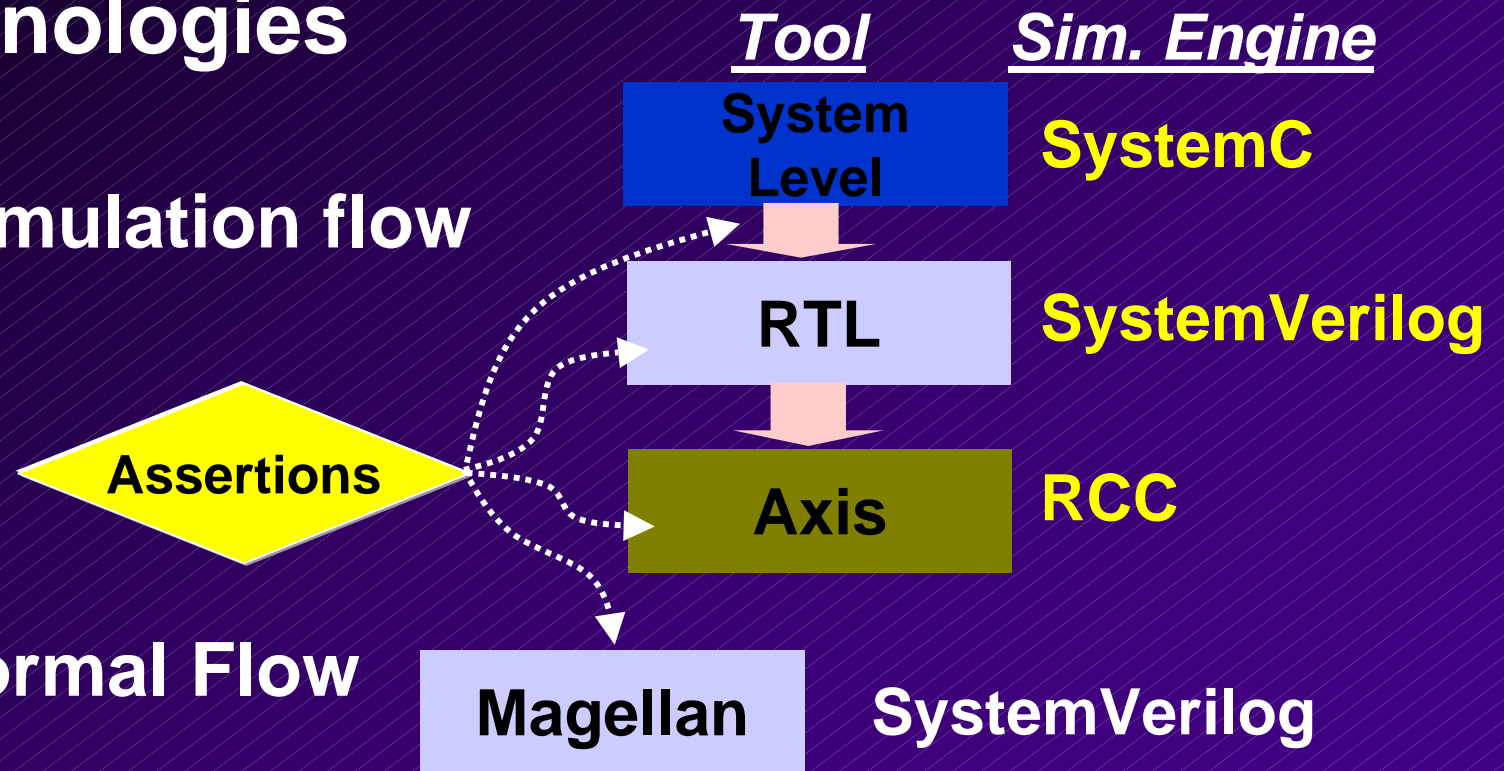


Powerful Verification Flow

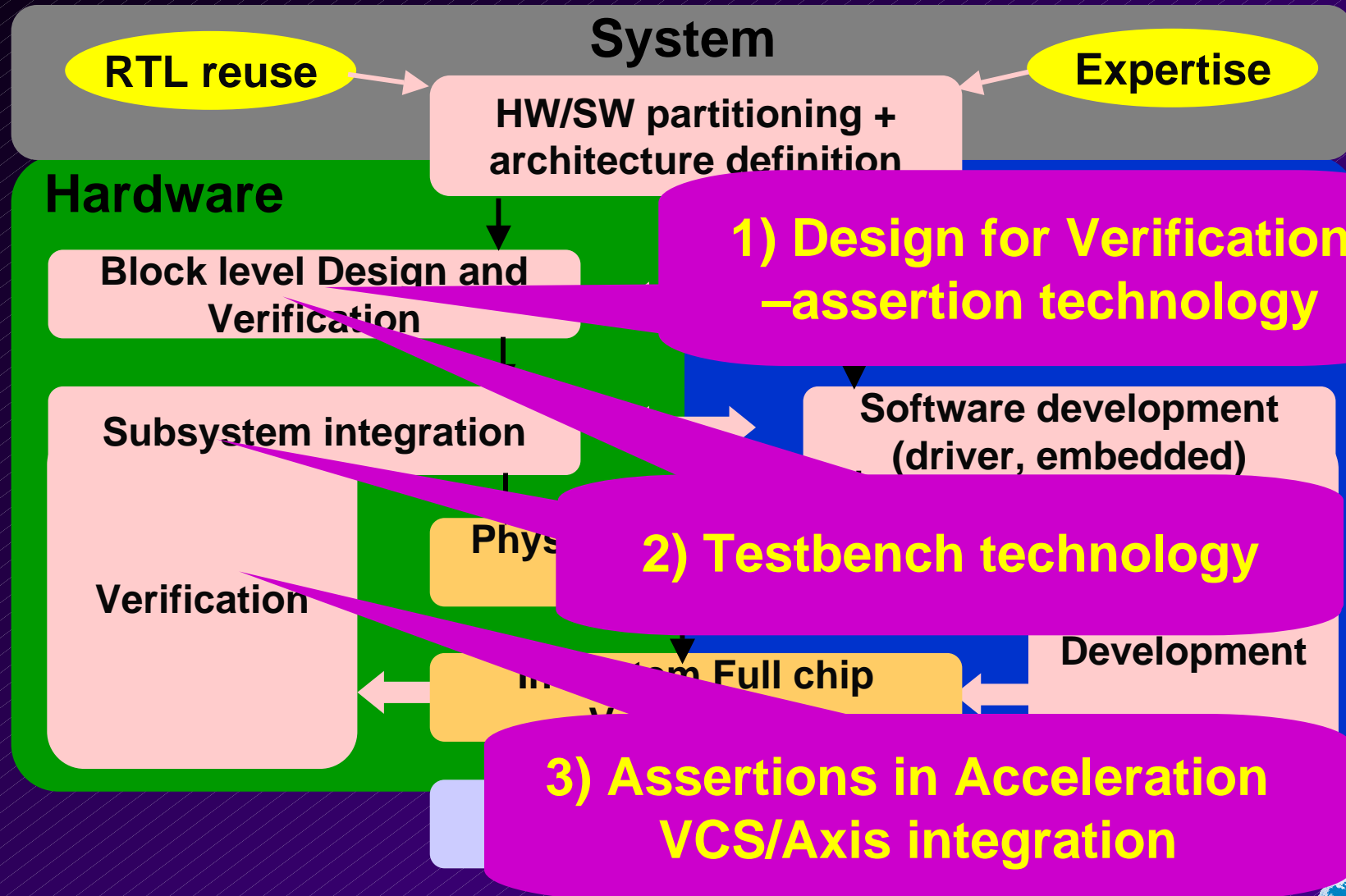
- Integration of best in class, proven technologies

- Simulation flow

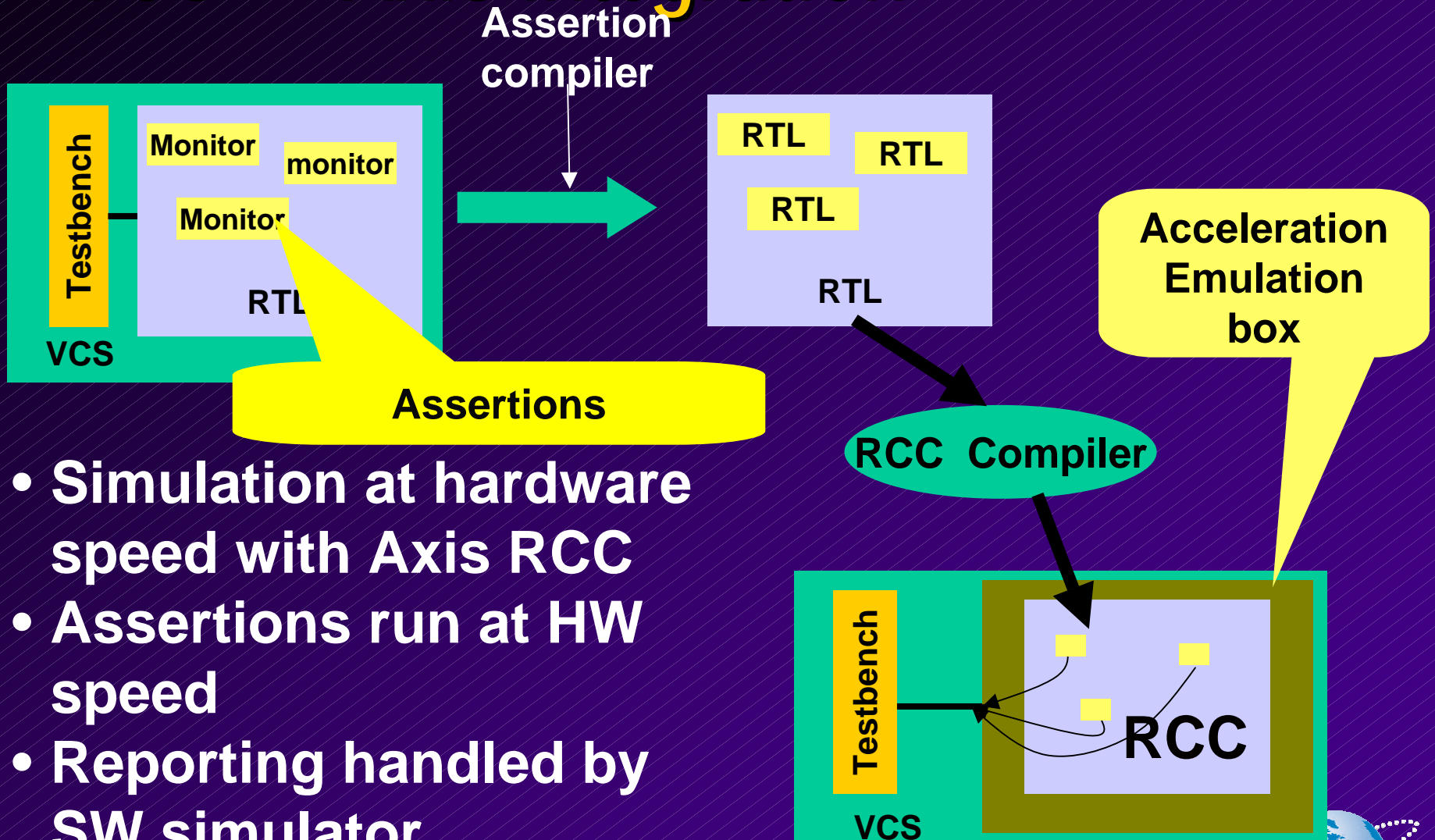
- Formal Flow



Next Generation Verification Flow



VCS ↔ Axis integration



- Simulation at hardware speed with Axis RCC
- Assertions run at HW speed
- Reporting handled by SW simulator



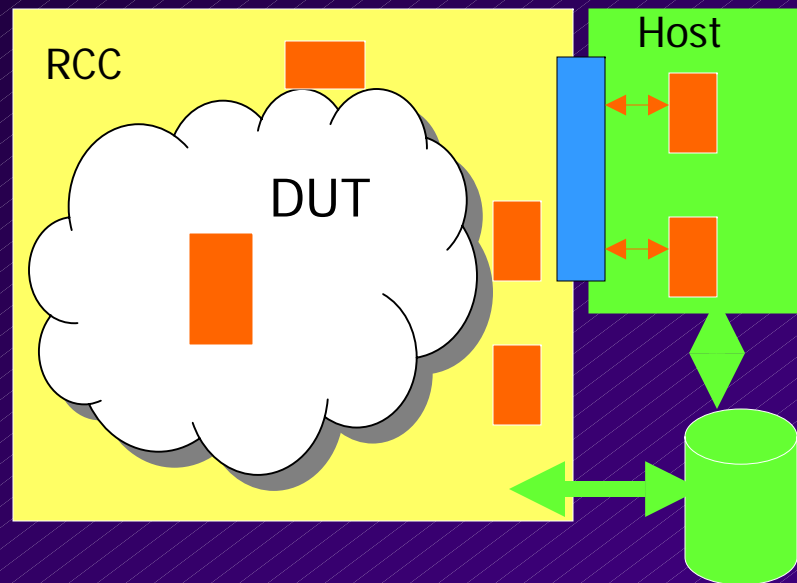
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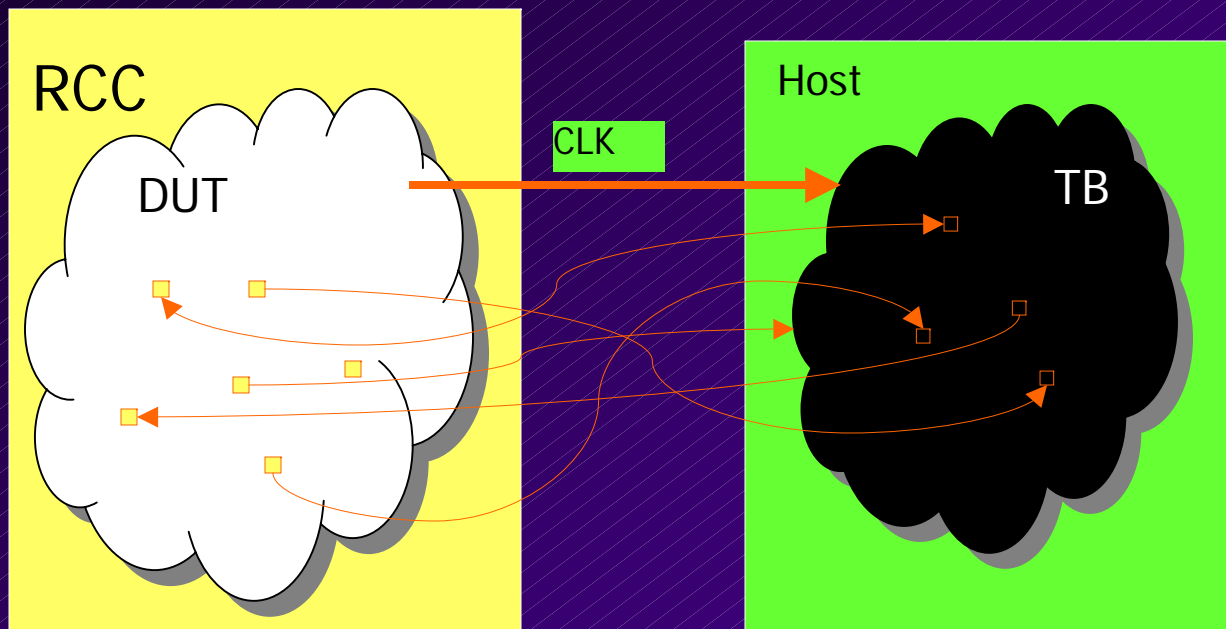
Test Bench: HDL (Verilog & VHDL)

- Transparent kernel integration
- Direct behavioral mapping + RPC host I/O
- Target-less Emulation



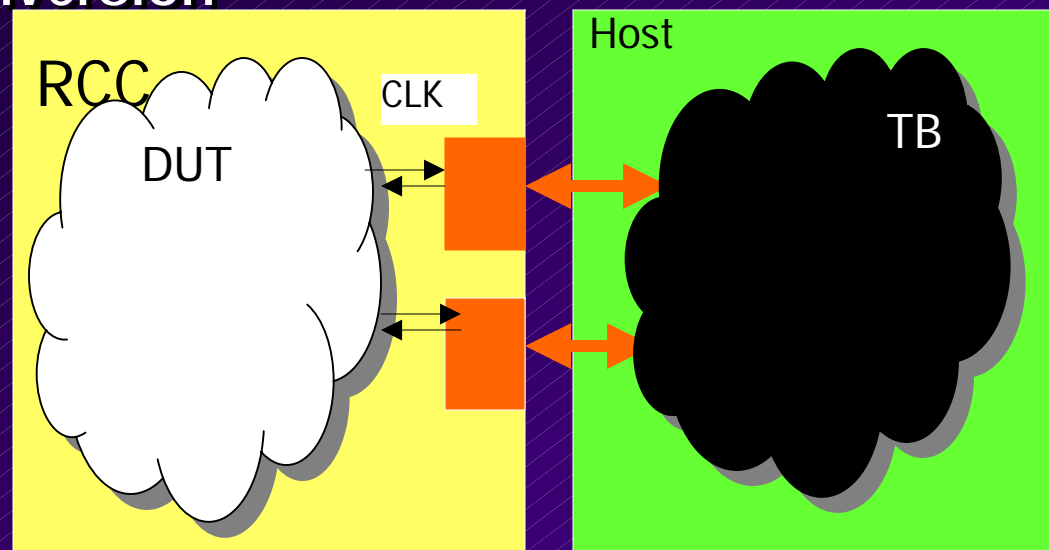
Test Bench: Co-Sim (C, Vera, e)

- Native support for PLI, VPI, VHPI and FLI.
- Multi-kernel sync overhead limits speed.



Test Bench: Transaction-based Co-Simulation (System C)

- Xbench: transactors in RCC
- Better performance by fewer synchronization
- Limited by Co-Sim synchronization and data object conversion



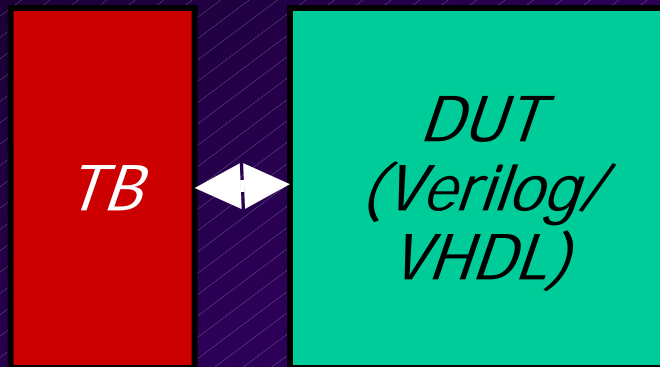
SystemVerilog Opens Acceleration Market

- What has Changed:
 - Testbench and assertions are embedded within the design
 - Sets natural boundary for testbench parallelism
 - Clear interface definition between testbench and design

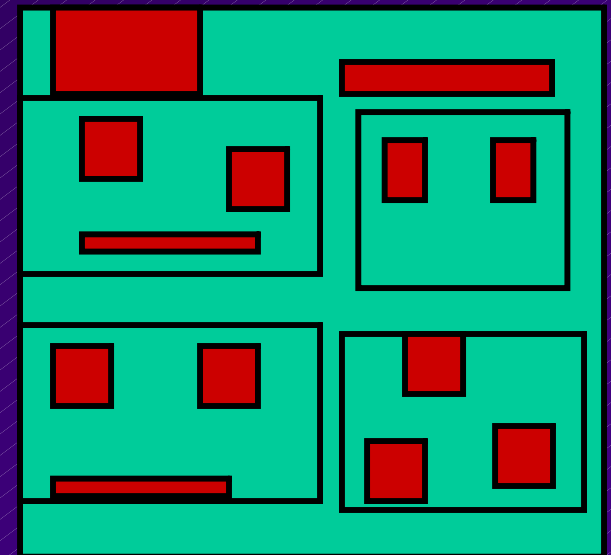


Embedded Testbench Activates Inherent Parallelism

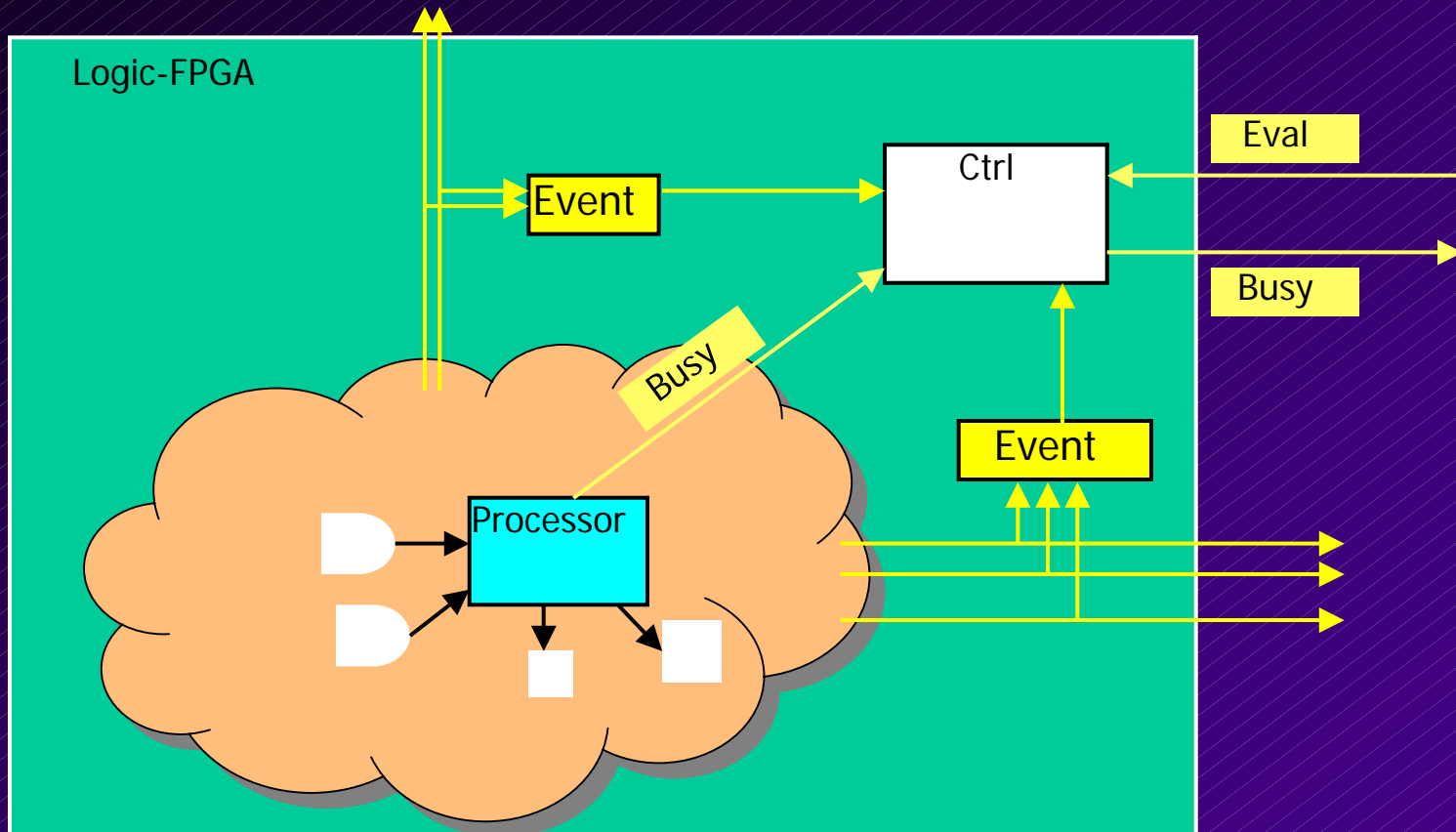
Now



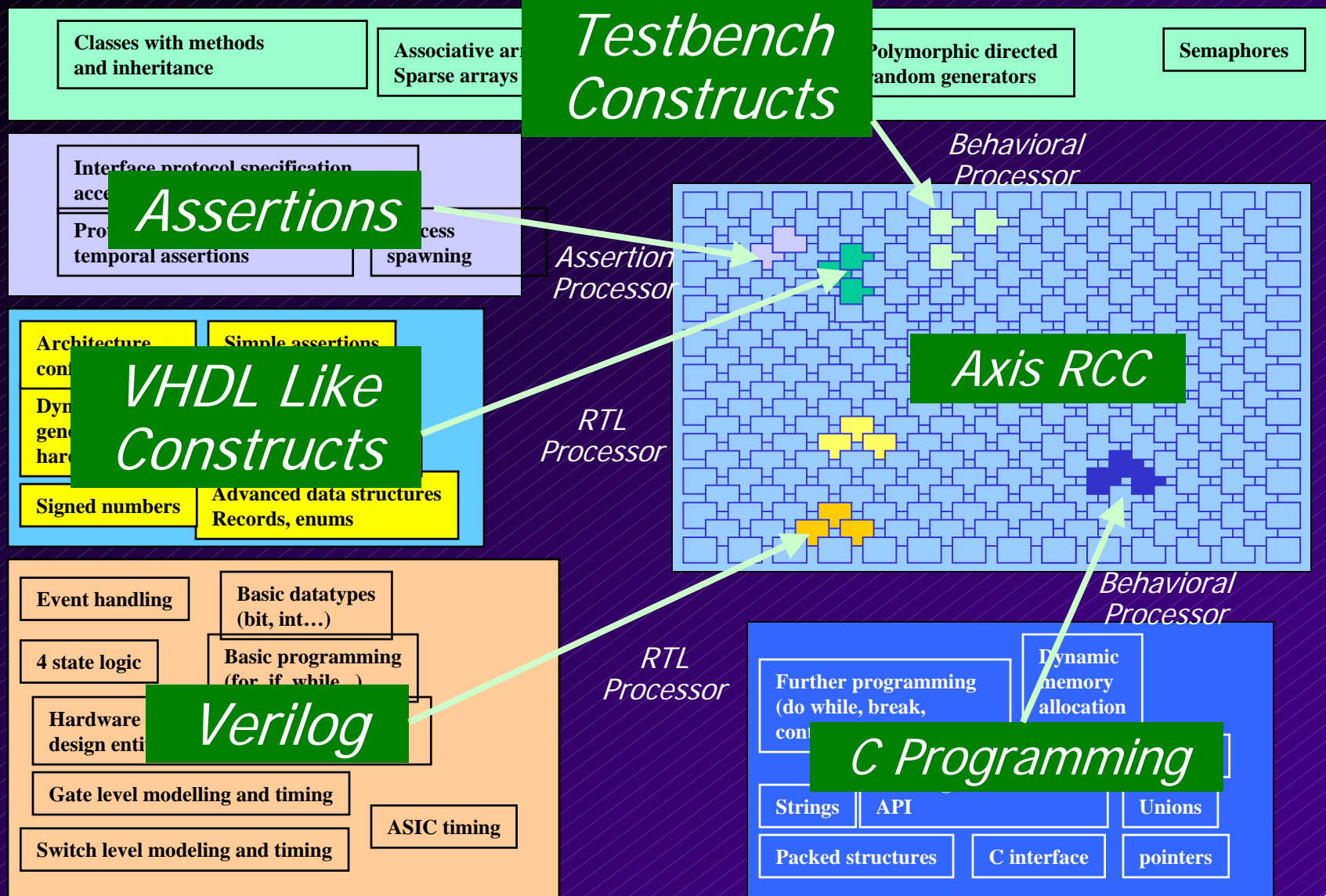
SystemVerilog



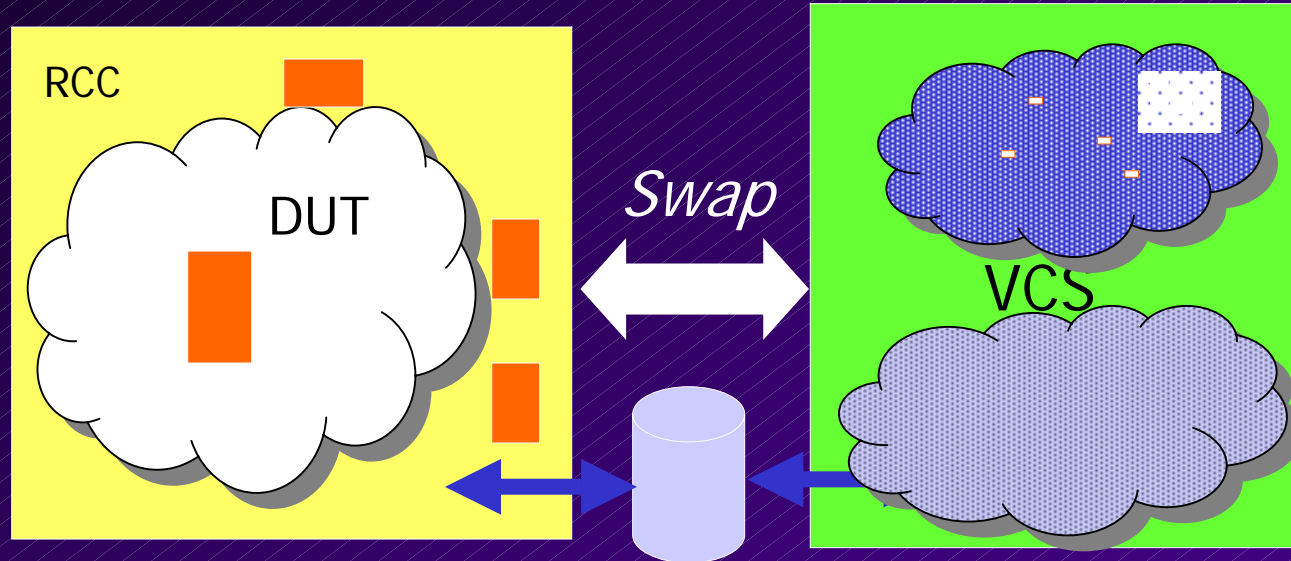
Direct Behavioral Modeling



SystemVerilog Accelerated on RCC



Full System Verilog Acceleration and Emulation



Summary

- Powerful integrated flow with VCS and Axis acceleration and emulation
- SystemVerilog changes simulation acceleration paradigm
- Axis' RCC behavioral processors can directly accelerate and emulate all SystemVerilog constructs

