



Accellera Update

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12th EDA Interoperability Developers' Forum

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Mission

Drive worldwide development and use of standards required by systems, semiconductor and design tools companies, which enhance a language-based design automation process.



Membership

- **Corporate**

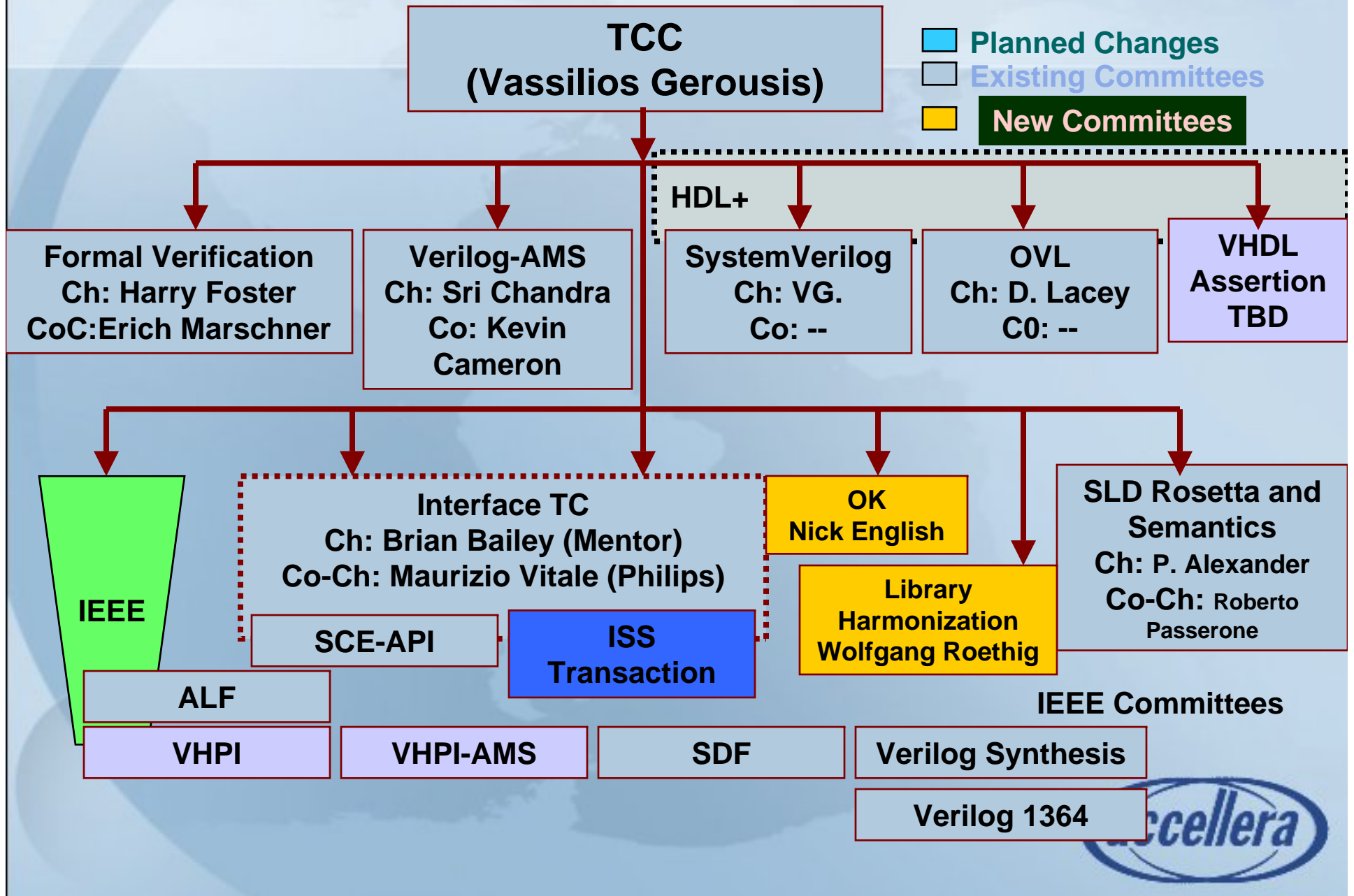
Axis Systems
ARM Ltd.
Artisan Components
Cadence Design Systems
IBM
Intel
Mentor Graphics
Motorola
NEC
Novas Software
NVIDIA
Real Intent
Sun Microsystems
Synopsys
Verisity

- **Associate**

0-In Design Automation
Galileo - a Marvell Company
Japan Electronics and
Information Technology
Association
Magma Design Automation
Sequence Design
ST Microelectronics
Toshiba
TNI - Valiosys



Accellera Technical Committees



Interfaces Technical Committee - ITC

Charter: Identify and standardize multi-abstraction and multi-domain interfaces that enable complete, high performance verification environments to be constructed.

- Formerly known as SCE-API
- Standard shipped - no reported issues so far
- Two commercial implementations now in the market
- Gathering requirements for next version



Library Harmonization

***Charter: Investigate library
harmonization and interoperability***

- ALF and Liberty
- Call for participation
- Contact Wolfgang Roethig

wroethig@necelam.com



Open Kit - OK

Charter: develop and promote a standard for design kits to enable and facilitate more efficient and automated custom IC design.

- 27 companies participating
- Design Objectives Document (DOD) ready for sharing
- Request donations to support DOD
- Contact Nick English

nenglish@cox.net



Open Verification Library - OVL

Charter: define, correct, enhance, and maintain the Open Verification Library of assertion templates. Templates provide an easy way to use assertions in Verilog and VHDL designs.

In progress:

- Support for SystemVerilog assertions
- Set up a bug tracker
- Create an improved testbench
- Correct inconsistencies with library semantics



Formal Verification - PSL

Charter: Develop and promote a Property Specification Language (PSL) compatible with Verilog and VHDL. Target both dynamic verification (e.g., simulation) as well as static verification (e.g., model checking).

- **PSL 1.1:**
 - Address issues raised in PSL 1.01
 - Correct errors and typos in PSL 1.01
 - Align with SystemVerilog assertions for same syntax and semantics
 - Consider extensions and proposals



Rosetta and System Level Semantics

Charter: Develop a standard syntax and semantics for Rosetta, a systems-level design language that addresses requirements specification for systems-on-chip designs.

- **Continuing work:**
 - Formal revision of language definition elements
 - Revision of domain semantics



SystemVerilog

Charter: Extend Verilog IEEE 2001 to higher abstraction levels for architectural and algorithmic design and advanced verification.

- **SystemVerilog 3.1a**
 - Address issues exposed in SystemVerilog 3.0/3.1 standard through implementation & usage
 - Address errata in SystemVerilog 3.1 standard
 - Add minor enhancements



Verilog-AMS and Device Model

Charter: Develop, update and promote analog and mixed signal extensions to the Verilog (IEEE-1364) language.

- In progress:
 - Cleanup activities for Verilog-AMS grammar
 - Investigating new features, enhancements, fixes
 - Device modeling updates
 - RF extensions investigation



More Goals for Coming Year

- Develop an enhanced process for building and maintaining standards with the IEEE
- Complete PSL 1.1 for unification with SystemVerilog 3.1a assertions
- Assign copyrights of SystemVerilog 3.1a to IEEE by DAC 2004
- Sync up Verilog-AMS with SystemVerilog digital syntax
- Drive another successful Design & Verification Conference

Join us !!

