

**SYNOPSYS®**

# Updates to SDC Open Source Format

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**> Your Interoperability Partner**

## Agenda

- Synopsys Design Constraints (SDC) Version 1.4 Enhancements
- SDC Parser Version 1.4 Update



## Update

- SDC version 1.4 is now available
- Design Compiler 2003.05, PrimeTime 2003.03 supports SDC 1.4
- SDC version 1.4 incorporates
  - 4 new commands
  - 13 new options/arguments of previously supported commands

## New SDC 1.4 Commands

- **set\_data\_check**

`set_data_check [-from from_object] [-to to_object] [-rise_from from_object] [-rise_to to_object]  
[-fall_from from_object] [-fall_to to_object] [-setup] [-hold] [-clock clock_object] value`

- **set\_max\_dynamic\_power**

`set_max_dynamic_power power [unit]`

- **set\_max\_leakage\_power**

`set_max_leakage_power power [unit]`

- **set\_min\_porosity**

`set_min_porosity [design_list] porosity_value`

## SDC Version 1.4 Enhancements

Support for the following “new” options to previously supported commands:

- `create_clock -add`
- `create_generated_clock -add`
- `create_generated_clock -master_clock`
- `set_driving_cell -min`
- `set_driving_cell -max`

## SDC Version 1.4 Enhancements (cont'd)

- `set_driving_cell -clock`
- `set_driving_cell -clock_fall`
- `set_input_transition -clock`
- `set_input_transition -clock_fall`
- `set_input_delay -network_latency_included`
- `set_input_delay -source_latency_included`
- `set_output_delay -network_latency_included`
- `set_output_delay -source_latency_included`

## SDC Parser Update

- SDC Parser version 1.4 and SDC 2003.03 documentation available for download at:  
[www.synopsys.com/tapin](http://www.synopsys.com/tapin)
- SDC Parser supports SDC 1.4, 1.3, 1.2, 1.1
  - SDC 1.3 is the default version for SDC parser





## Download Open Source SDC 1.4 and Use It Now!

- Update your tools to SDC version 1.4 and remain current with other EDA vendors and your customers
- For SDC support questions use the following:
  - [sdc@synopsys.com](mailto:sdc@synopsys.com)
- For TAP-in program general information contact:
  - [tap-in@synopsys.com](mailto:tap-in@synopsys.com)

A stylized, blue-tinted graphic of a circuit board or chip, positioned in the lower-left quadrant of the slide.

[www.synopsys.com/tapin](http://www.synopsys.com/tapin)

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