

SILICON METRICS

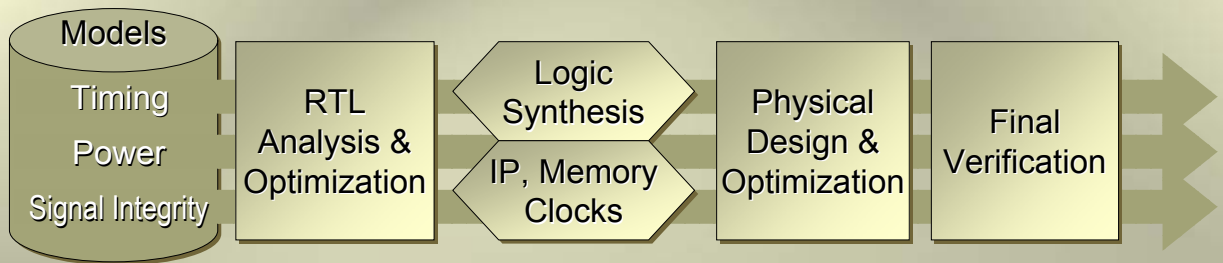
Characterization Considerations for Static Noise Analysis

Robert Jones – Dir. Strategic Marketing

Spring 2003 Developers' Forum

Models Drive Design, Analysis and Verification

Nanometer Process Technologies Drive the Need for Retooling



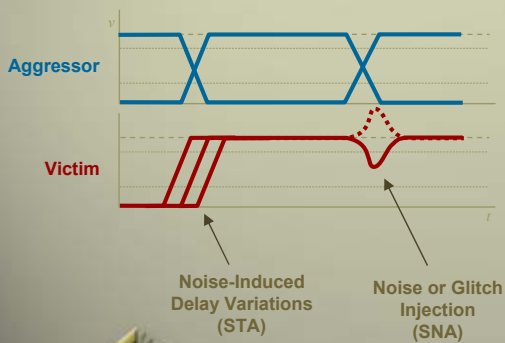
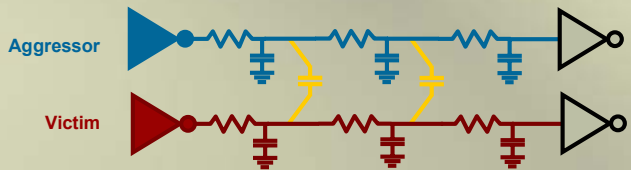
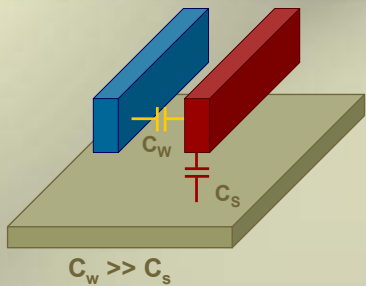
The Impact of Nanometer Process Technologies

- Reduced Cell Delays with Tighter Stable Operating Regions
- Increasing Leakage Currents and Hidden Power Sources
- **Increased Capacitive Coupling Causing Signal Noise**
- Smaller Noise Margins for Greater Rail Voltage Sensitivity
- More Data to Analyze During Shorter Design Cycles
- Smaller Staffs with Stretched Beyond Domain Expertise



Signal Integrity In Nanometer Design

Analyzing the Impact of Capacitive Cross Coupling



- ⇒ Lower Performance
 - ◆ Victim Delay Degradation
- ⇒ Functional Failures
 - ◆ Hold Violating Speedups
 - ◆ Captured Data Glitches



Supporting Static Noise Analysis Tools

New Modeling for Key Static Noise Analysis Components

- ◆ **New Static Noise Tools Reduce Time to SI Closure**
 - Advanced Analysis Addresses False Positives Problem
 - Requires Additional Model Data for More Complete Analysis
- ◆ **New Models Require New Characterization**
 - Vendors Extend Libraries With Noise Constructs
 - Supplements Existing Timing & Power Constructs

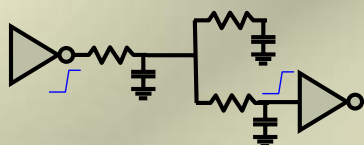
Algorithm Component	General Model Requirement
Injected Glitch Calculation <ul style="list-style-type: none">• Determine initial noise waveform injected on a non-switching victim.	Improved Driver Model
Glitch Sensitivity Evaluation <ul style="list-style-type: none">• Determine functional (and reliability) impact of noise.	Noise Sensitivity Model
Glitch Waveform Propagation and Combination <ul style="list-style-type: none">• Determine noise amplification or attenuation propagated along paths.	Noise Propagation Model



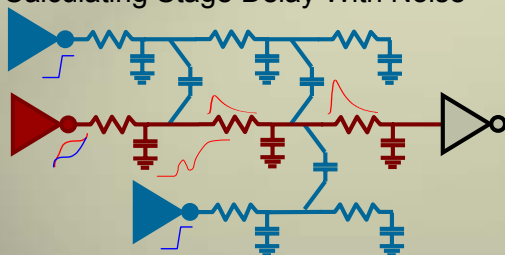
Improved Driver Models for Noise Analysis

Modeling for Crosstalk Delay and Injected Glitch Calculations

Calculating Stage Delay Without Noise



Calculating Stage Delay With Noise

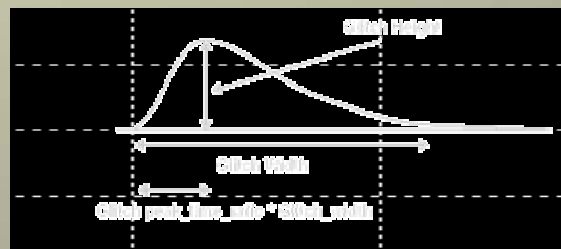
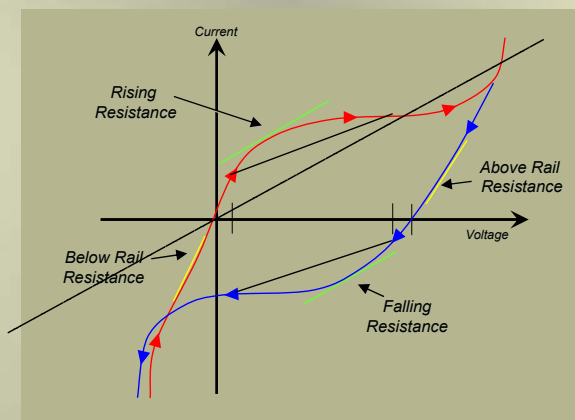


- ◆ Better Models Needed for Crosstalk
 - More Complex Networks Analyzed
 - More Complex Waveforms Modeled



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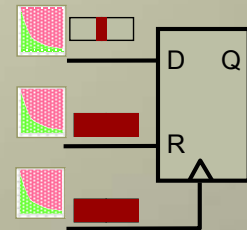
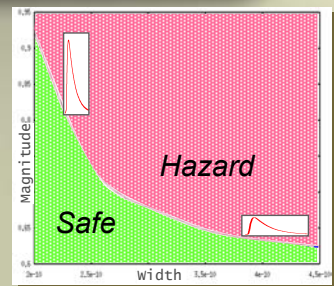
Steady State Driver Modeling



Noise Evaluation of Glitch Sensitivity

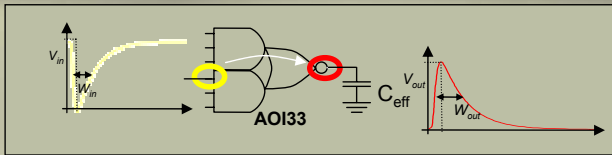
Advanced Modeling for the Impact of Glitch Waveforms

- ◆ Glitch Sensitivity Critical to Analysis
 - Determines Hazardous Glitch Energy Levels
 - *Hazard* Indicates an Erroneous Output Response
 - Applied to Combinational & Sequential Pins/Arcs
- ◆ Functional Hazard Checking
 - Focused on Between Rail Glitches
 - Glitch Size Checked on State Critical Pins
 - Filtered by Setup/Hold Noise Window for D Inputs
 - Always Critical (No Window) for Async & Clocks
 - Indicates Functional Failure If Captured
- ◆ Reliability Hazard Checking
 - Includes Above & Below Rail Glitches
 - Protects Against Reliability Issues
 - Used to manage combinational glitches

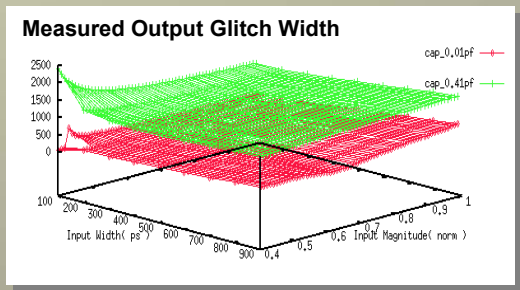
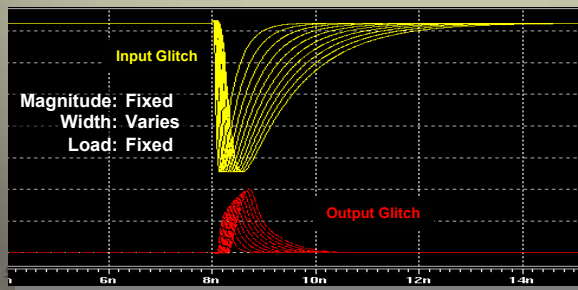
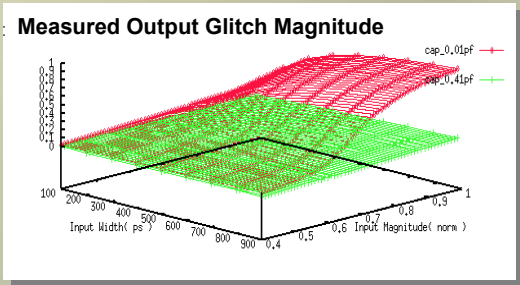
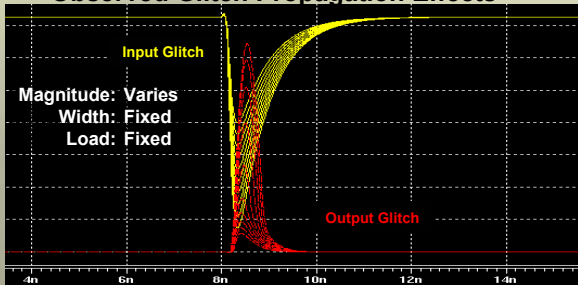


Modeling Glitch Propagation Through Cells

Eliminating Pessimism in Crosstalk Noise Analysis



Observed Glitch Propagation Effects



SI Characterization Considerations

Raw Simulations for Signal Integrity v. Timing & Power

Cell	Timing & Power	Signal Integrity									
		Improved Driver	Noise Immunity			Noise Propagation		Added Simulation Totals by SI Modeling Level			
			I-V	2-D	3-D	3-D	4-D	1	2	3	4
Comb_4	896	80	560	3,920	2,744	10,976	80	640	3,384	14,976	
Comb_6	1,344	120	840	5,880	4,116	16,464	120	960	5,076	22,464	
Comb_9	2,016	180	1,260	8,820	6,174	24,696	180	1,440	7,614	33,696	
Comb_11	3,136	280	1,960	13,720	9,604	38,416	280	2,240	11,844	52,416	
Seq_N	1,308	30	630	4,410	1,029	4,116	30	660	1,689	8,556	
Seq_S	2,832	60	1,400	9,800	2,058	8,232	60	1,460	3,518	18,092	
Normalized:	100%						10%	80%	400%	1500%	
SI Modeling Level 1:		✓									
Level 2:		✓	✓								
Level 3:		✓	✓		✓						
Level 4:		✓	✓	✓	✓	✓					



Modeling Tradeoff for Static Noise Analysis

Impact of Characterization Decisions on Analysis Capability

			Static Noise Analysis Capability by SI Modeling Level				
			Level 1	Level 2	Level 3	Level 4	
Noise Delay			✓	✓	✓	✓	Calculates crosstalk delay impact on switching victim signal during timing analysis.
Noise Injection			✓	✓	✓	✓	Calculates the waveform for a noise glitch injected on to quiescent victim network.
Noise Evaluation	Stage Based	DC	✓	✓	✓	✓	Analyzes noise sensitivity at the sink device of a victim network using only glitch magnitude.
		Glitch M&W		✓	✓	✓	Analyzes noise sensitivity at the sink device of a victim network using glitch magnitude and duration.
	Path Based	Glitch M&W			✓	✓	Analyzes noise sensitivity on an overall path basis by adding propagation of noise waveforms.
		Glitch Shape				✓	Analyzes noise sensitivity on an overall path basis with combinational propagation of noise waveforms using more detailed shape descriptions.



SI Characterization: Defining the Challenge

What Library Providers Need to Roll Out Support for SNA

◆ The Challenge

- Several New & Unfamiliar Constructs To Support
- Multiple Tools & Flows To Support
- Significant New Characterization Overhead
- Limited Resources to Deploy New Libraries

◆ Solution Requirements

- Must Meet Real SI Needs for Today's Design Teams
- Must Seamlessly Support Popular Tools
- Must Help Library Developers Get To Market Quickly
- Must Provide Growth Path as Model Needs Evolve
- Must Be Cost Effective Total Solution



The SiliconSmart SI Solution

Advanced Characterization & Modeling for 130nm Design

◆ Ready – Satisfy Designer Needs Now

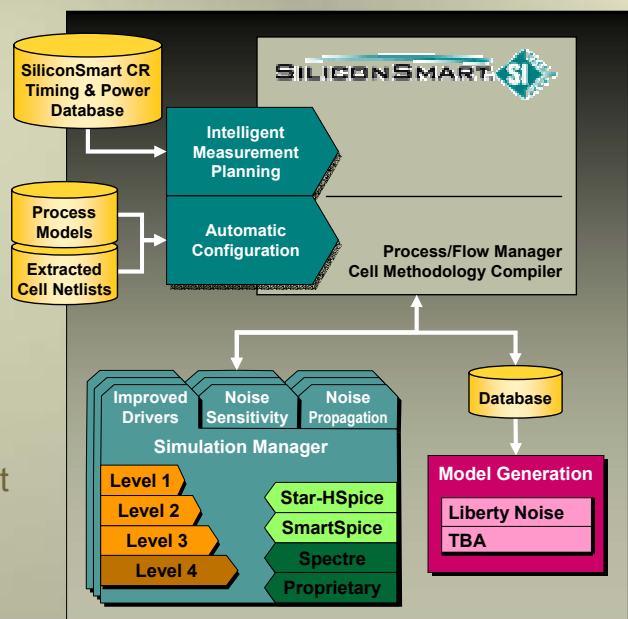
- 1st Complete SI Modeling Product
- Supports PrimeTime SI 2003.03 Noise Analysis
- Installed at Major Customers

◆ Proven – Deploy with Confidence

- Chosen by Leading Lib Providers
- Jointly Developed & Certified With Synopsys & TBA
- Founded on the Characterization Leader's SiliconSmart Technology

◆ Practical – Minimize Total Rollout Cost

- High-Throughput Incremental Solution
- Flexible Modeling Support Levels
- Consistency Across Multi-Platforms



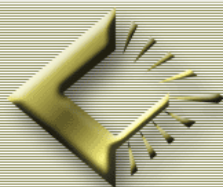
Intelligent Measurement Planning

Flexibility to Accelerate SI Characterization

	Timing & Power	Added Simulation Totals by SI Modeling Level			
		1	2	3	4
Raw Simulation Counts	100%	10%	80%	400%	1500%
With Intelligent Measurement Planning	100%	10%	25%	100%	400%

- ◆ Intelligent Measurement Planning Accelerates SI Characterization
 - Uses Existing Timing Database to Identify Optimum Noise Measurements
 - Characterization Throughput for Level 3 Noise Equals Timing & Power
- ◆ Using Level 3 Noise Models Accelerates Design Closure
 - Provides Stage-Based Filtering Using Load-Dependent Noise Immunity
 - Provides Glitch Propagation Models for Path-Based Glitch Filtering





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