

Accellera: What, Why & How



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Accellera Introduction

- What is Accellera?
- Why does Accellera work?
- How does it help you?



What is Accellera?

- Accellera is a non-profit electronics industry organization that drives the worldwide development and use of standards required by systems, semiconductor and design tool companies that enhance a language-based design automation process.
- For more information, please visit:
www.accellera.org
- For a list of Accellera-supported activities, visit:
www.accellera.org/subcom.html



Current Membership

- 0-In Design Automation
- **Axis Systems, Inc.**
- **Cadence Design Systems**
- Galileo – a Marvell Company
- JEITA
- **IBM**
- Intel
- Magma Design Automation
- **Mentor Graphics**
- **Motorola**
- **NEC**
- **Novas Software**
- **Real Intent**
- Sequence Design, Inc.
- ST Microelectronics
- **Synopsys**
- **Sun Microsystems**
- **TransEDA**
- **Verisity**
- **Verplex**

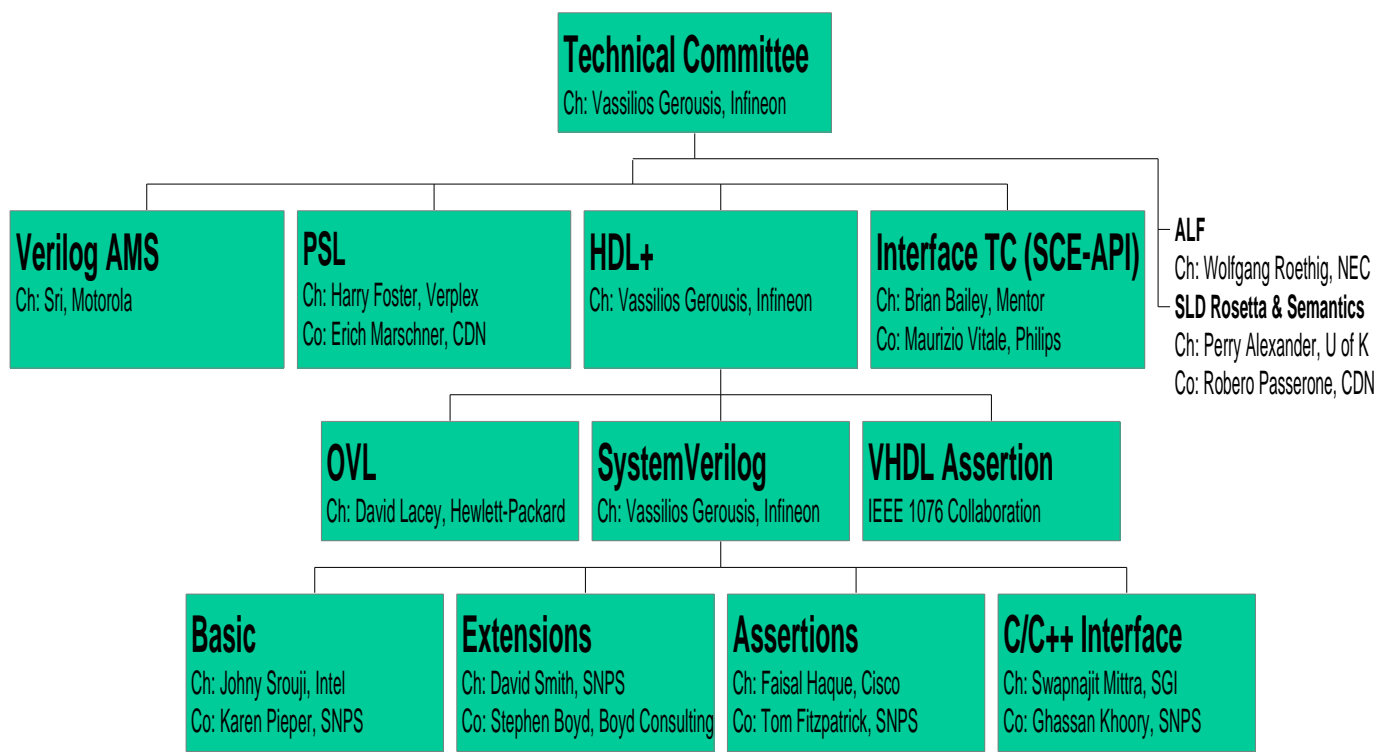


Accellera' History

- Open Verilog International
 - IEEE 1364-1995, 1364-2001 Verilog HDL
 - IEEE 1497 SDF (used by 1364 & 1076.4)
 - Verilog AMS
- VHDL International
 - IEEE 1076 VHDL and related standards
 - IEEE 1076.4 VITAL
 - IEEE 1499 Open Model Interface
- Joint Projects
 - IEEE 1481 Delay & Power Calculation System (also with Si2)
 - RTL Synthesis Interoperability Standards
 - > IEEE 1076.6 & IEEE P1364.1
 - IEEE P1603 ALF



Accellera Present & Future



Accellera Supports the IEEE

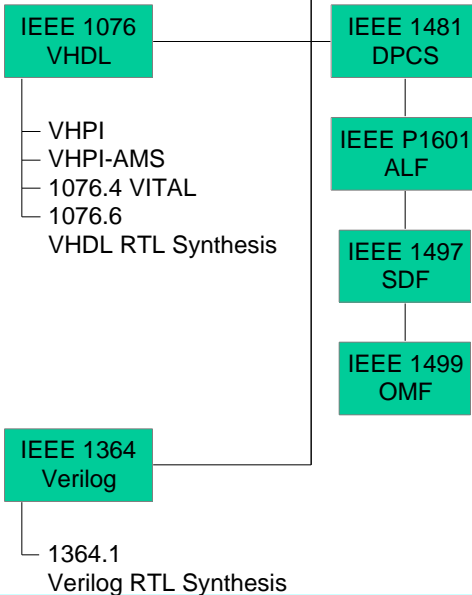


Accellera
Technical Committees



IEEE Computer Society
DASC

- Accellera forwards completed standards to the IEEE
- Accellera supports on-going IEEE work



Why Accellera Works



- It supports and obeys the fundamental EDA laws



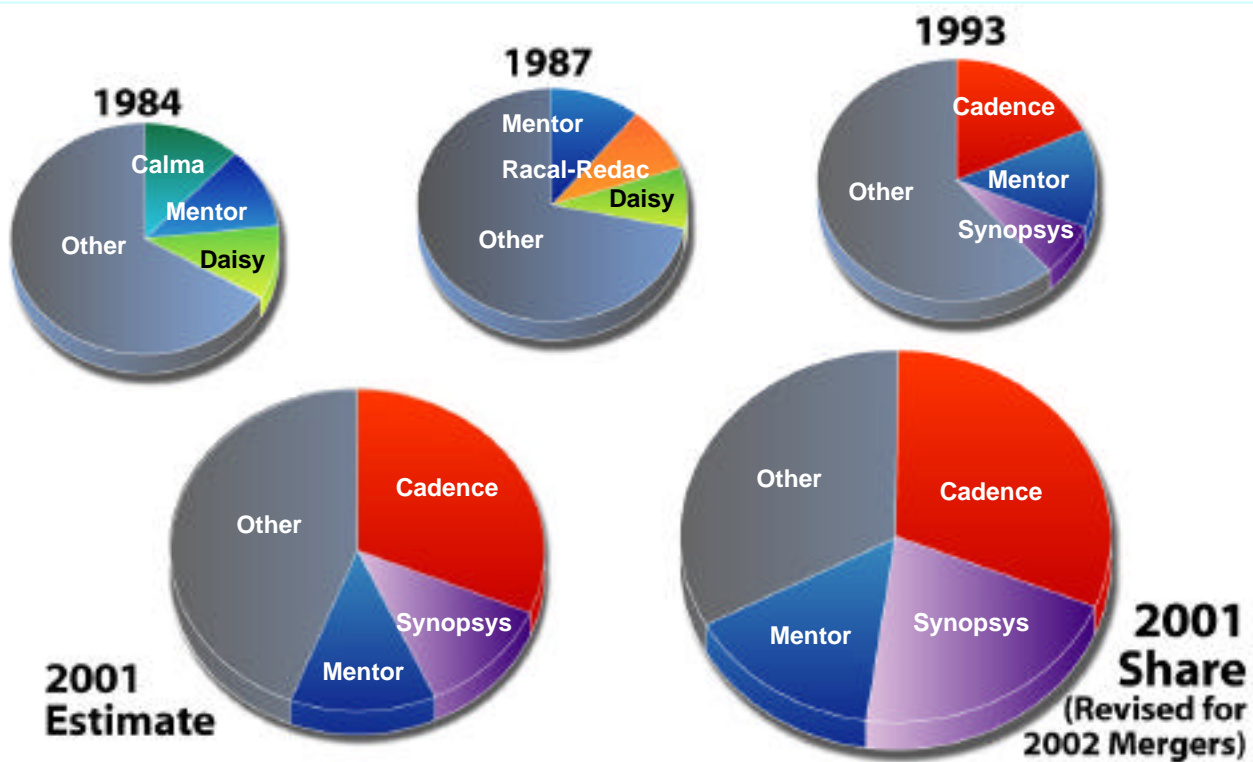
Fundamental Law #1



**There are Always Three
Large EDA Companies
and Many Small Ones.**



Always Three Large EDA Players



Accellera Supports Business Imperatives

Build standards from known commercial donations connected to industry business demands.

- Verilog
 - Donated by Cadence
- SPEF
 - Donated by Cadence
- PDEF
 - Donated by Synopsys
- Verilog-AMS
 - Donated by Cadence
- OMF
 - Donations from Synopsys & Cadence
- ALF
 - Donations from Mentor, Cadence & others
- SystemVerilog
 - Donations from Co-Design, Real Intent, 0-In & Synopsys
- OVL
 - Donated by Verplex
- PSL
 - Donations from IBM, Motorola, Verisity & Intel
- ITC (SCE-API)
 - Donated by IKOS



Fundamental Law #2



SINGLE VENDOR
Integrated Solutions
Always Fail.

MULTI VENDOR
Interoperability
Always Wins.



The Framework Era: 1989-1992

- EDA companies drive single vendor integrated environments built around frameworks
- Major standardization organization
 - The CAD Framework Initiative -
- Supported by users for interoperability between software applications



Colossal failure – users wanted interoperability, not single vendor control



Accellera Facilitates Interoperability

- Interoperability Supported
 - Specifications well documented to reduce or eliminate ambiguity of interpretation
 - Complete and full standardization path to IEEE for globally certified standard
- Accelerate multi-company adoption
 - Testcases
 - Parsers
 - When necessary, reference implementations
 - And more...



Fundamental Law #3



**Growth in Design Creation
Productivity Drives
Growth in Need
for Design Verification.**

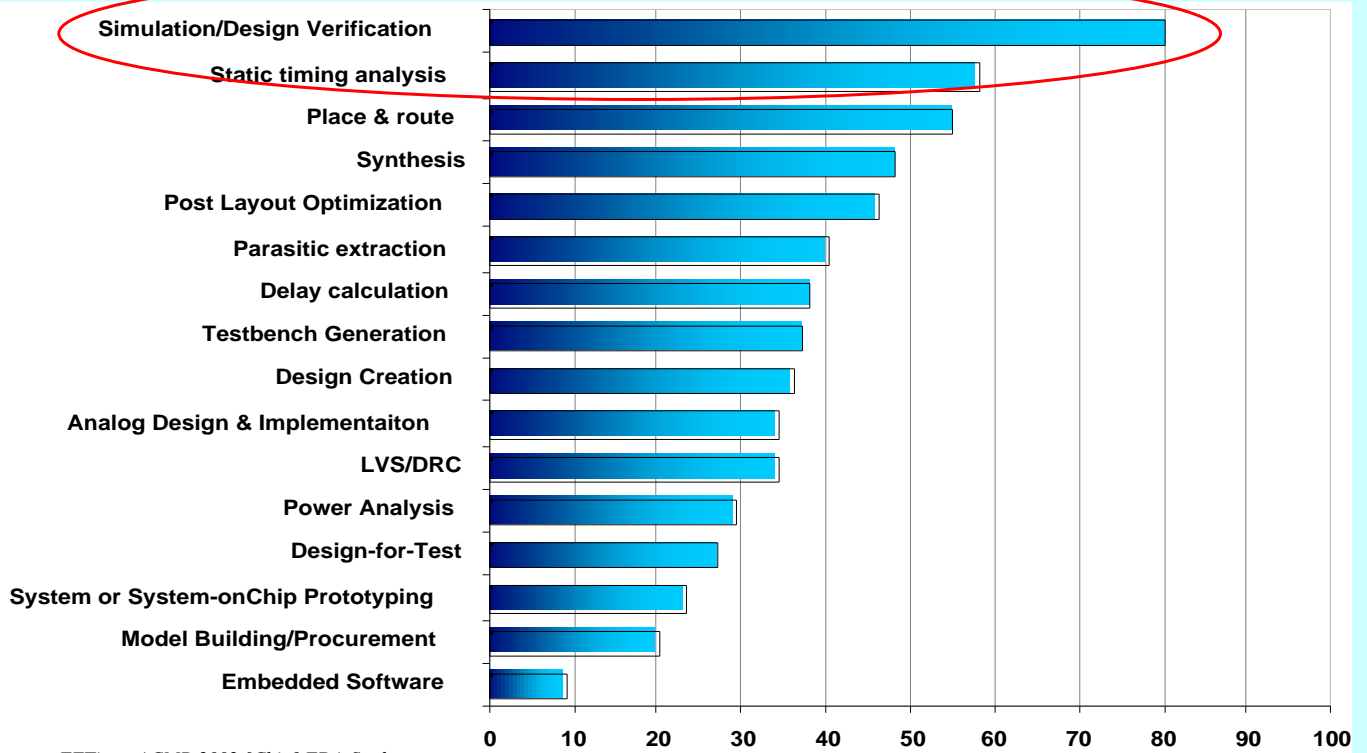


High Level Design Drives New Methodologies 1992-1997

- Adoption of HDLs and logic synthesis
- Productivity increases with higher level of abstraction
 - IP reuse, Design reuse, Platform-based design ...
 - Automated synthesis
- Growth of physical design tool market



Verification is the Bottleneck



Sources: EETimes / CMP 2002 [Chip] EDA Study



Accellera Drives Productivity

- SystemVerilog address design & verification
 - Design Creation Productivity through SystemVerilog Synthesis
 - Design Verification Productivity through SystemVerilog Verification
 - System & Architectural modeling enhanced
 - > SystemVerilog C Data Types
 - > SystemVerilog Direct Programming Interface (DPI)
- ITC (SCE-API) standardizes high-speed transaction interface for advanced verification
- PSL opens exploration of next generation formal technology



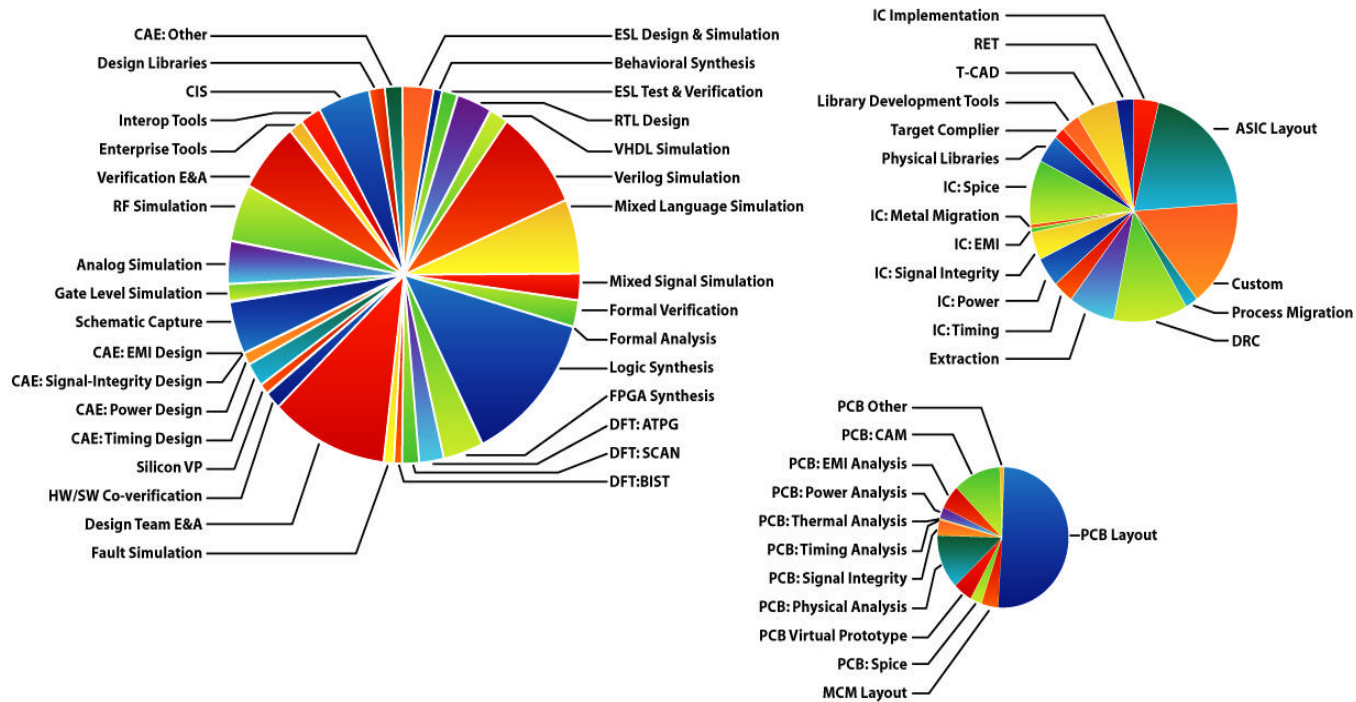
Fundamental Law #4



**Increased Specialization
and Economies of Scale
Always Win.**



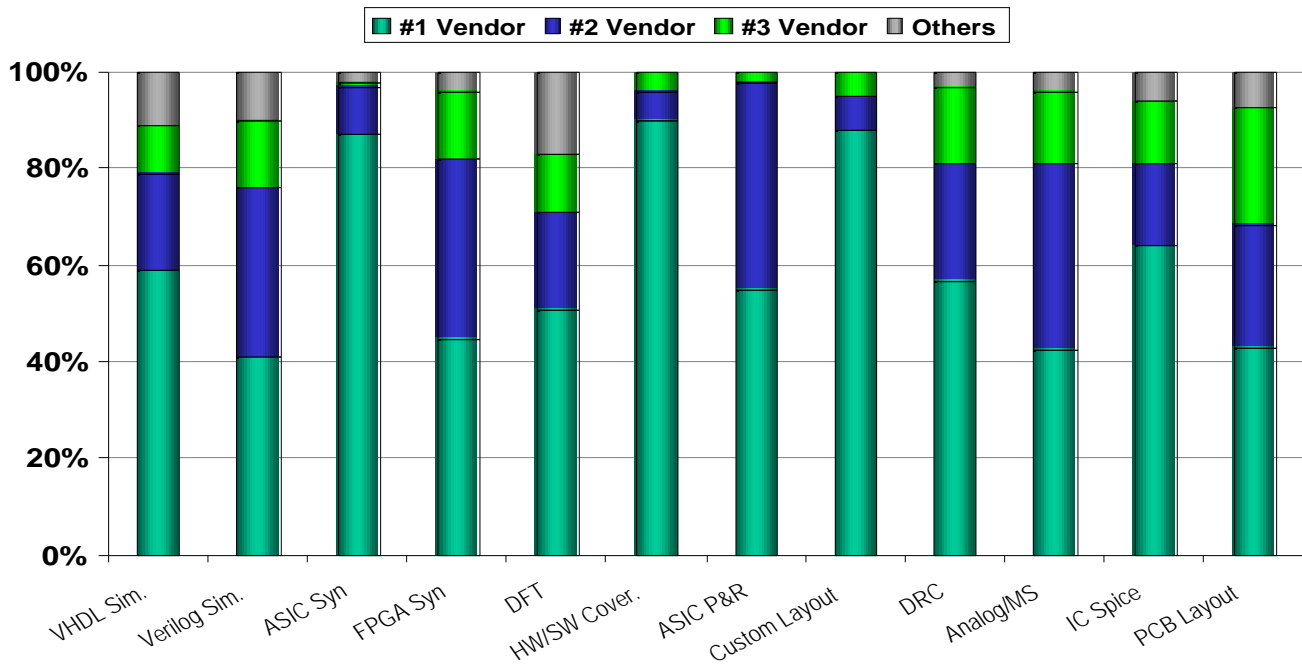
No Vendor Can Be “Best in Class” for Every Segment of EDA



Source: Dataquest Market Trends, October 2001



Every Large EDA Segment Has a 40%+ Owner



Accellera Works with EDA Segment Leaders

- Accellera membership is balanced
 - Systems Companies
 - Semiconductor Companies
 - EDA Companies
 - > Small
 - > Medium
 - > Large
- Donations generally come from EDA Segment Leaders



Summary – Obeying the Laws



There are Always Three Large EDA Companies and Many Small Ones.

Accellera: Be relevant to the Large Three



Single Vendor Integrated Solutions Always Fail.

Accellera: Users want interoperability; address it.



Growth in Design Creation Productivity Drives Growth in Need for Design Verification.

Accellera: Invest in Design & Verification Std's: SystemVerilog



Increased Specialization and Economies of Scale Always Win.

Accellera: Work with all; seek Donations from leaders



How does Accellera help you?

- In General
 - Protects Users with EDA product choices
 - > Increased number of product implementation choices
 - > Competition on algorithm implementations offers quality choices
 - You can participate and drive standardization to meet your business needs
 - > Your design methodologies augmented with open standards
 - Standards approach ensures efficiency
 - > Specification is authority for interpretation
 - > Reduces number of interoperability bugs
 - > Interoperability of tools can be done at your site
 - Facilitates global trade
 - > Builds markets (IP, Design Re-use, Platform design)



How Does Accellera Help You?

- Specifically
 - Addressing Verification Crisis
 - SystemVerilog – the new Hardware Design & Verification Language
 - PSL unified with SystemVerilog
 - Interconnect Technology – to connect other verification components like HW/SW design systems, Instruction Set Simulators, Emulators, Accelerators, and more ...
 - Verilog AMS – Permit digital and analog to be verified within the context of one language.



Conclusion

- Standards ...
 - Build markets
 - Underpin design processes
 - Protect consumers
 - Support trade
 - Spread benefits of innovation
- Staffed by volunteers ...
 - You can become one too!
 - See www.accelera.org for more information

