

Analog / RF Design  
Flows

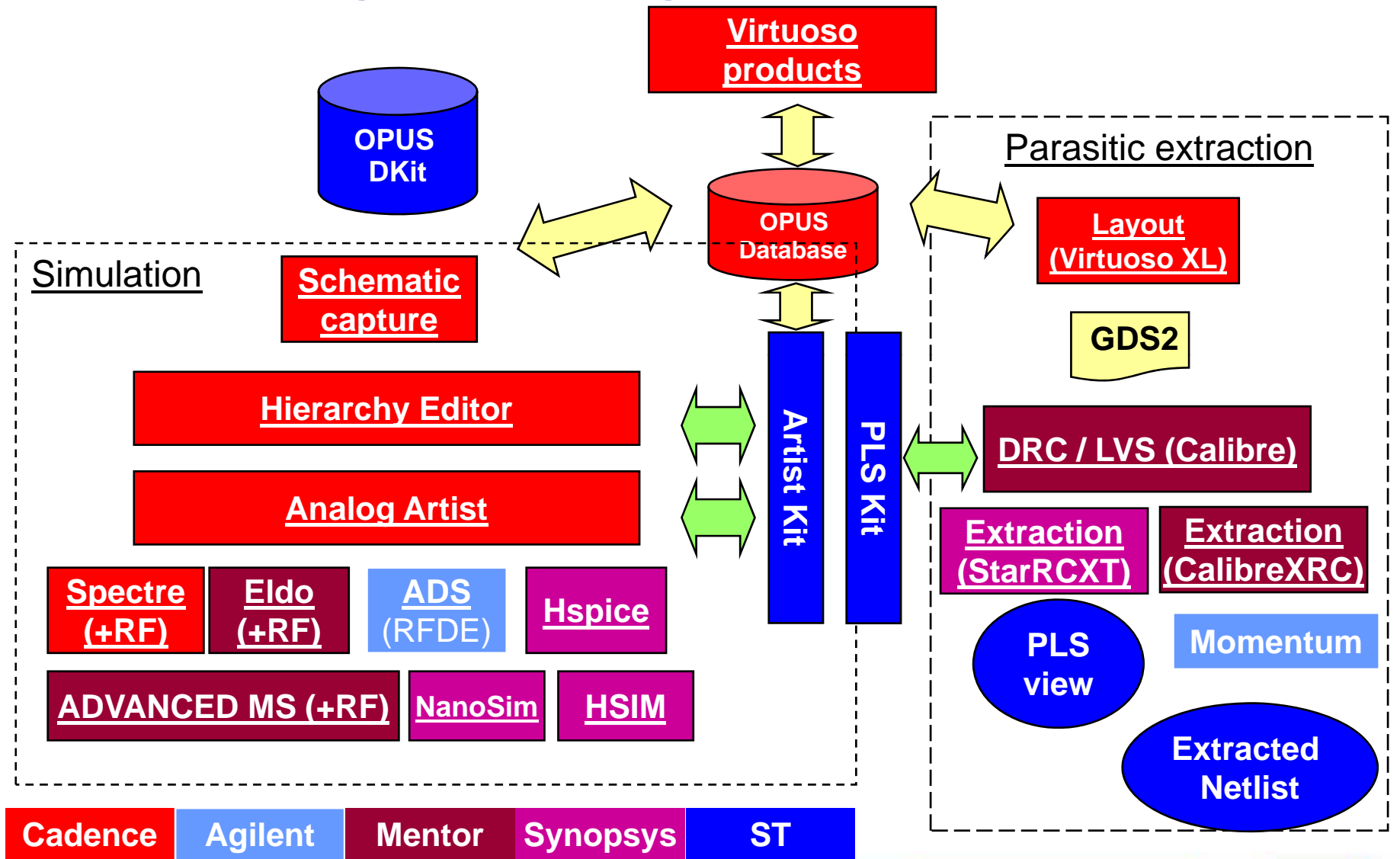
Status/Directions



Central CAD  
& Design Solutions

Philippe  
MAGARSHACK

# ST Analog/RF design environment



# Multiple design teams

IP blocks may come from several different groups or companies, with different CAD flows



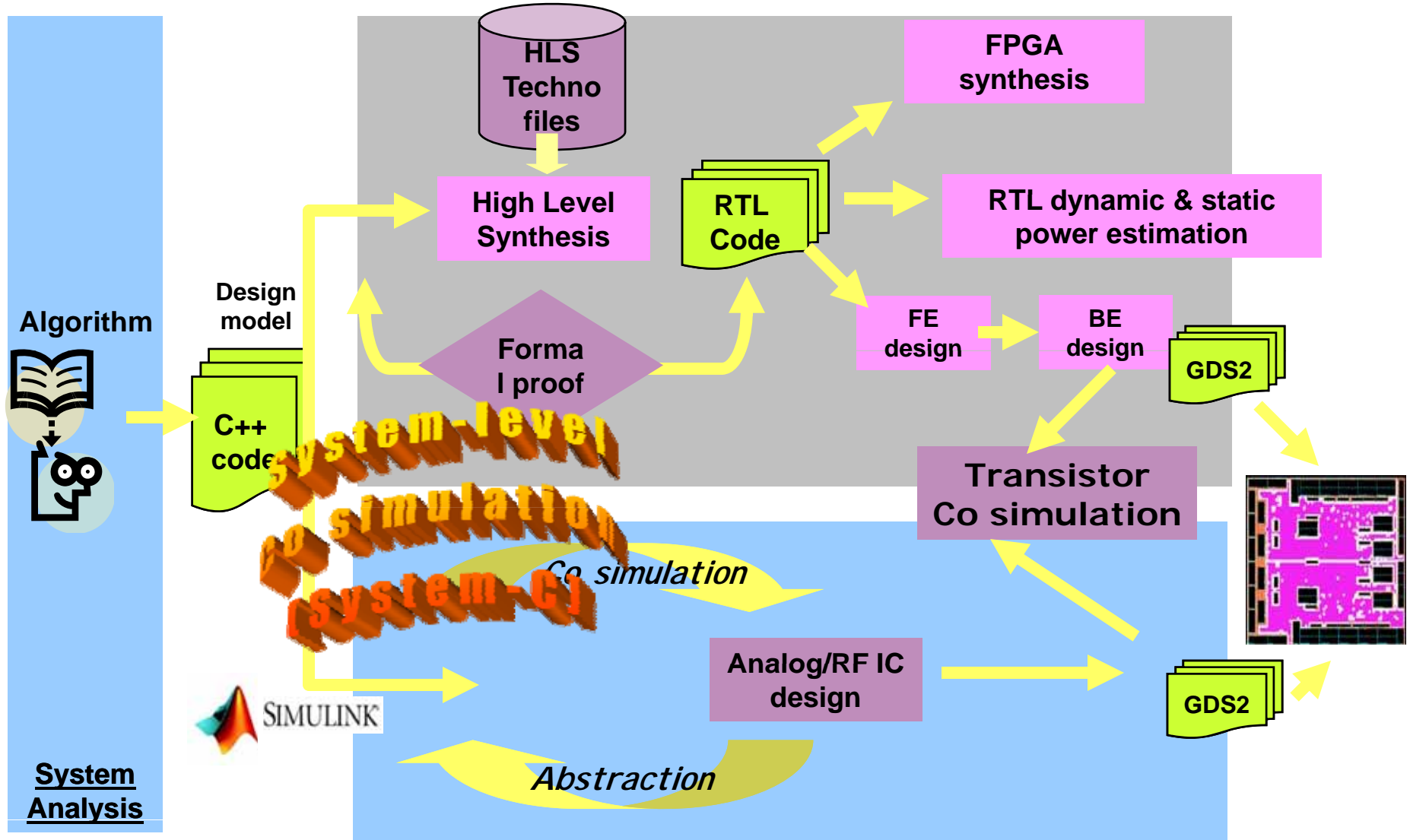
**Agilent Technologies**  
Innovating the HP Way

Today:



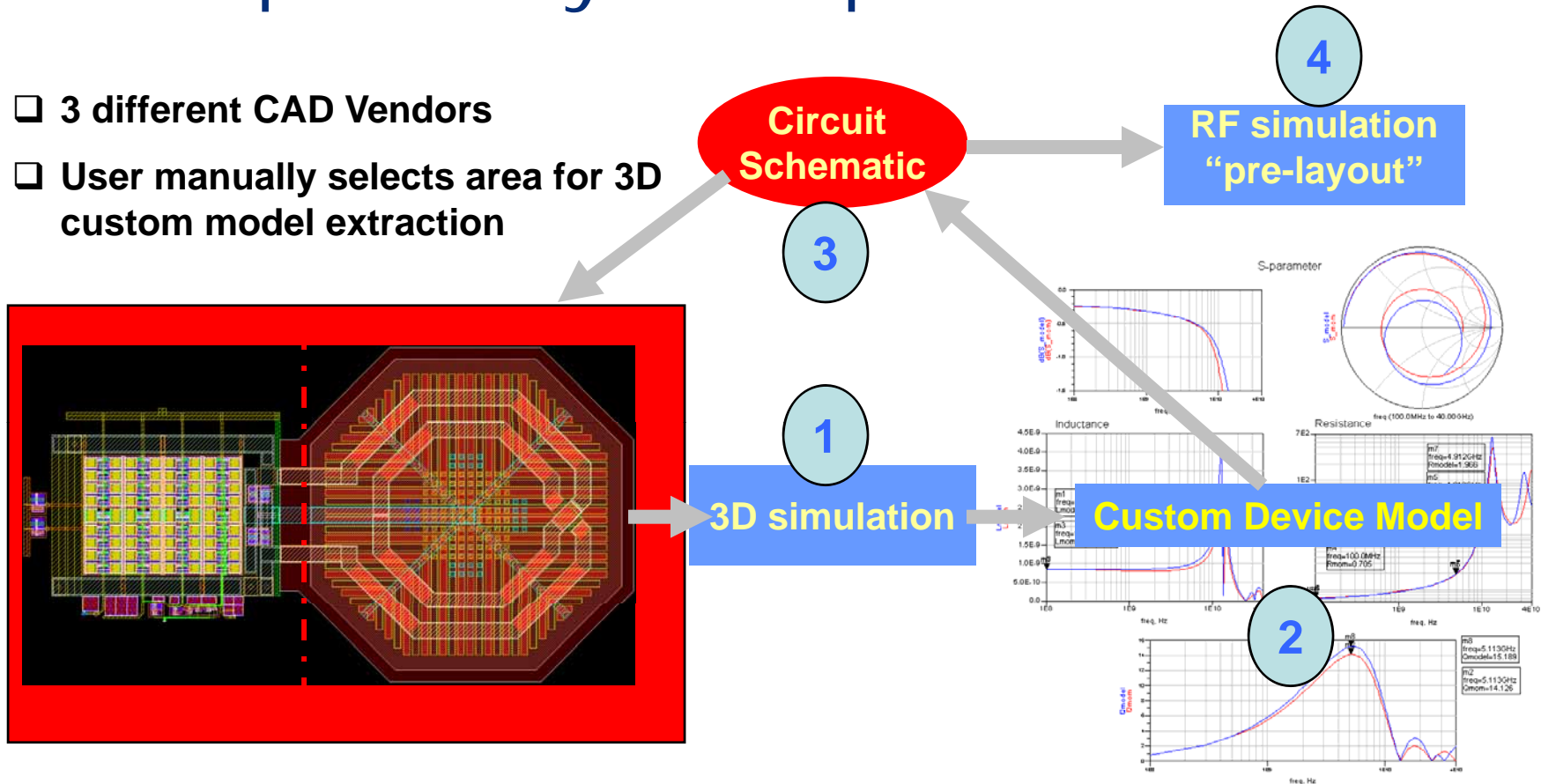
Plus many CAD resources!!!

# Interoperability example in RF



# Interoperability example in RF IP

- ❑ 3 different CAD Vendors
- ❑ User manually selects area for 3D custom model extraction



Cadence

Agilent

Synopsys

ST

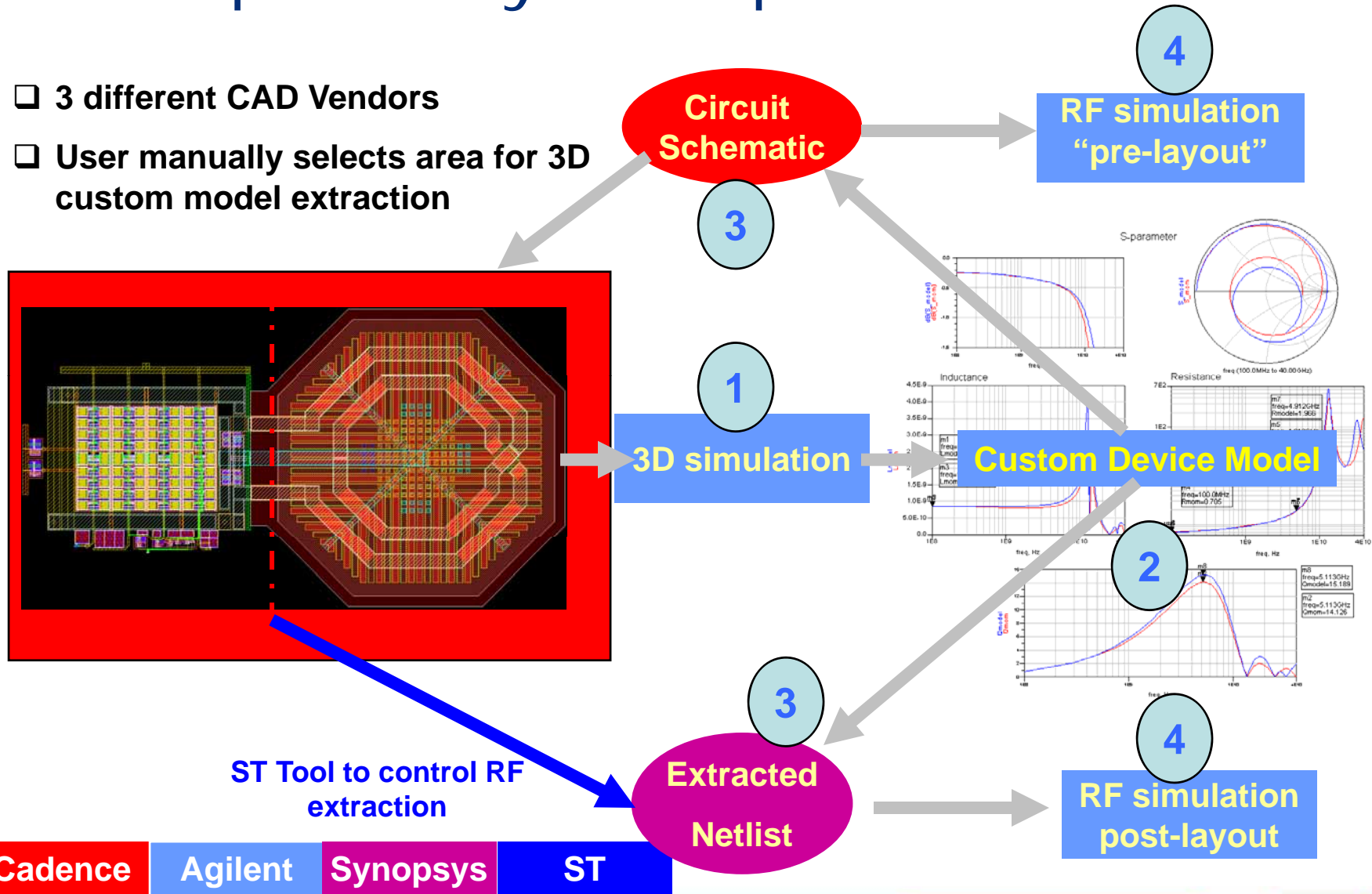
11/06/2008

DAC 2008



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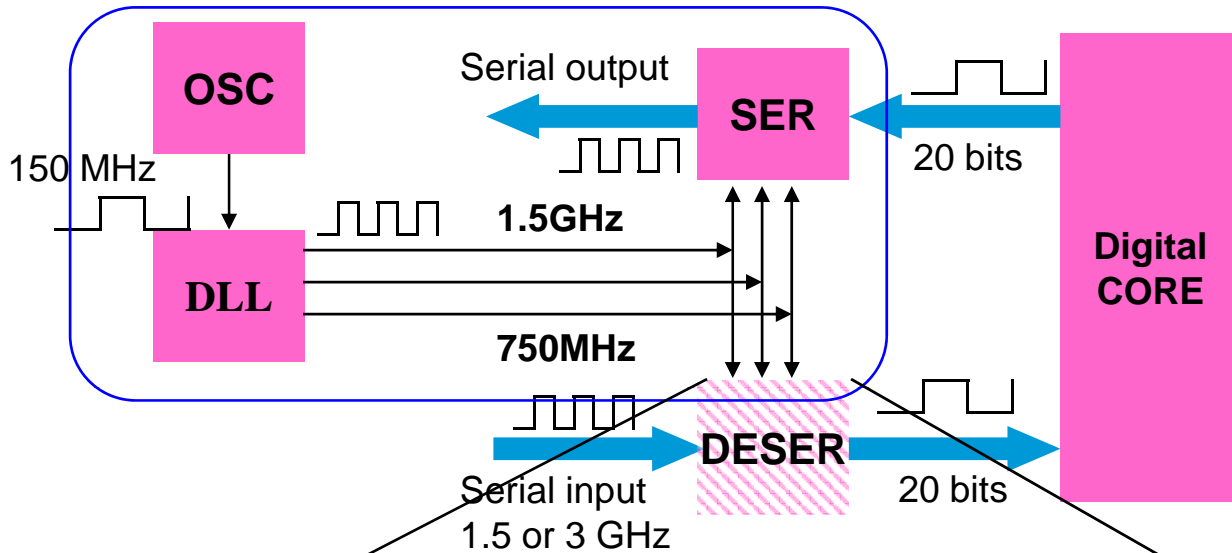
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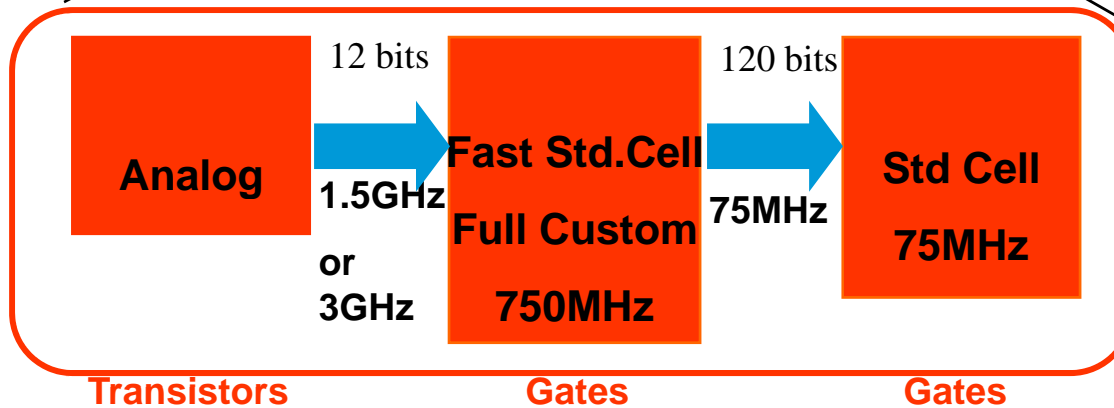


# SERDES I/O : Mixed-signal Design

## Top level Macro (extracted without parasitics)



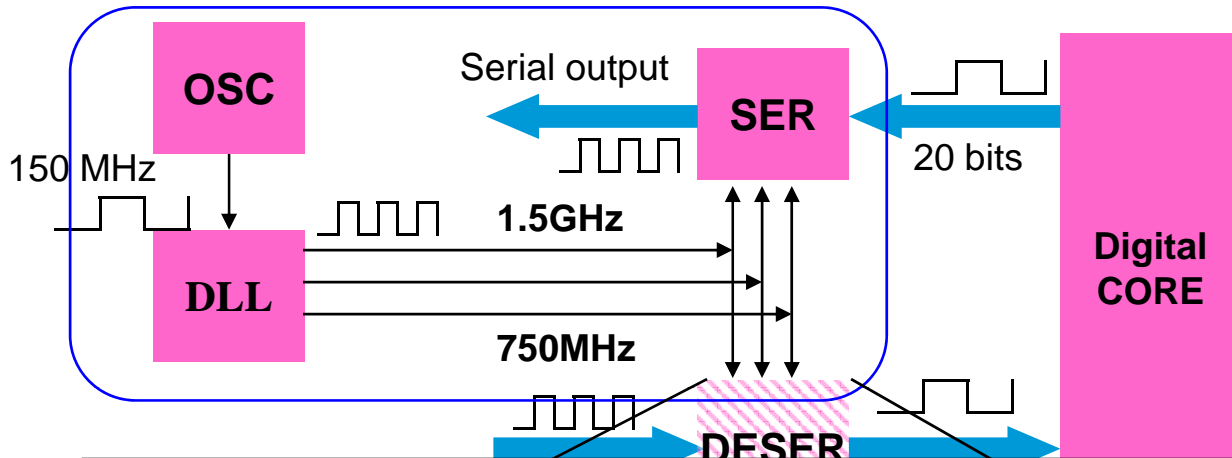
## RC extracted netlist



- ▣ **Mixed mode** RC extraction
  - ▣ Wires with RC
  - ▣ Wires with C only
- ▣ **Hierarchical LVS**
  - ▣ hierarchical extracted netlist
- ▣ **Skip** non-critical blocks
  - ▣ speed-up simulation
- ▣ **back-annotate DSPF**
  - ▣ to layout 0-RC netlist
- ▣ Run **Hsim** or **Hsim-NCsim**
- ▣ **Timing checks** for Flip-Flops:
  - ▣ Built-in Hsim command `.tcheck setup / hold ...`

# SERDES I/O : Mixed-signal Design

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  - Wires with RC
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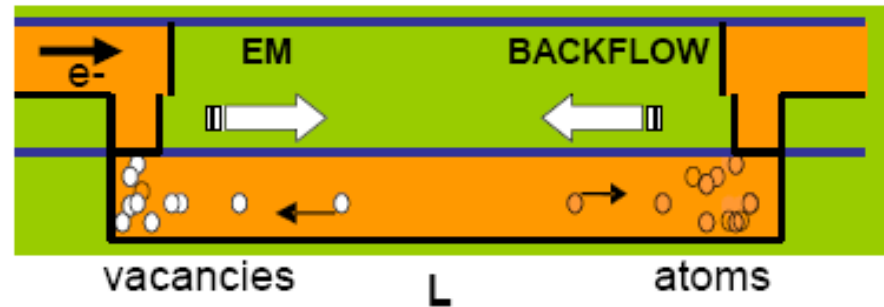
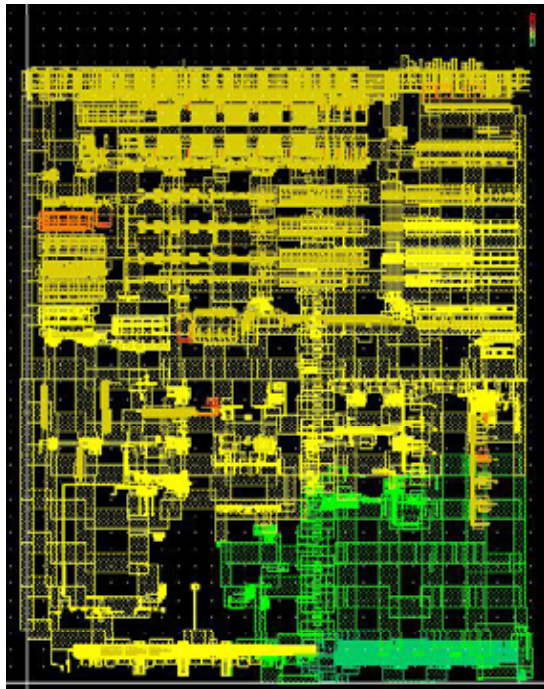
Lot of manual actions

Lot of vendors specific tricks

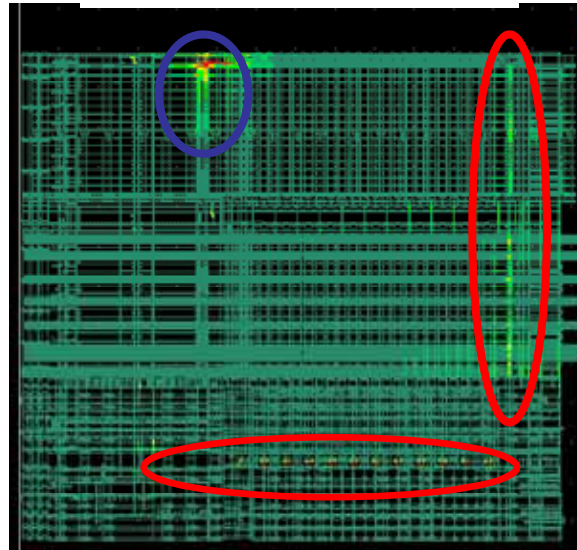


# Interconnect Reliability

IRdrop



Electro-migration



Required a strong collaboration between EDA and Technologists for optimal modeling (Blech, Aging, ...) -> **Proprietary Blech-Equations Format(s)!!!**

# Standardization At Device level

- 📄 **Modeling: open thanks to CMC**
  - 📄 Verilog-A : interoperable at 98% → what about the 2% ???
  - 📄 No standard to describe process variations (Device, Metals)
    - 📄 → impact on methodology: custom- $\sigma$ , Design of Experiments (Custom Simulation Space), ...
- 📄 **Waveform display – Waveform analysis: No standard!**
  - 📄 There is only one BEST tool in the world ... but EACH EDA company has one !
- 📄 **Static/Dynamic netlist Check: No standard!**
  - 📄 No standard at all (even within single vendor!!!! )
- 📄 **PCells: open thanks to OA**
  - 📄 Many 3<sup>rd</sup> party vendors 😊

THANK YOU



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