

Analog / RF Design
Flows

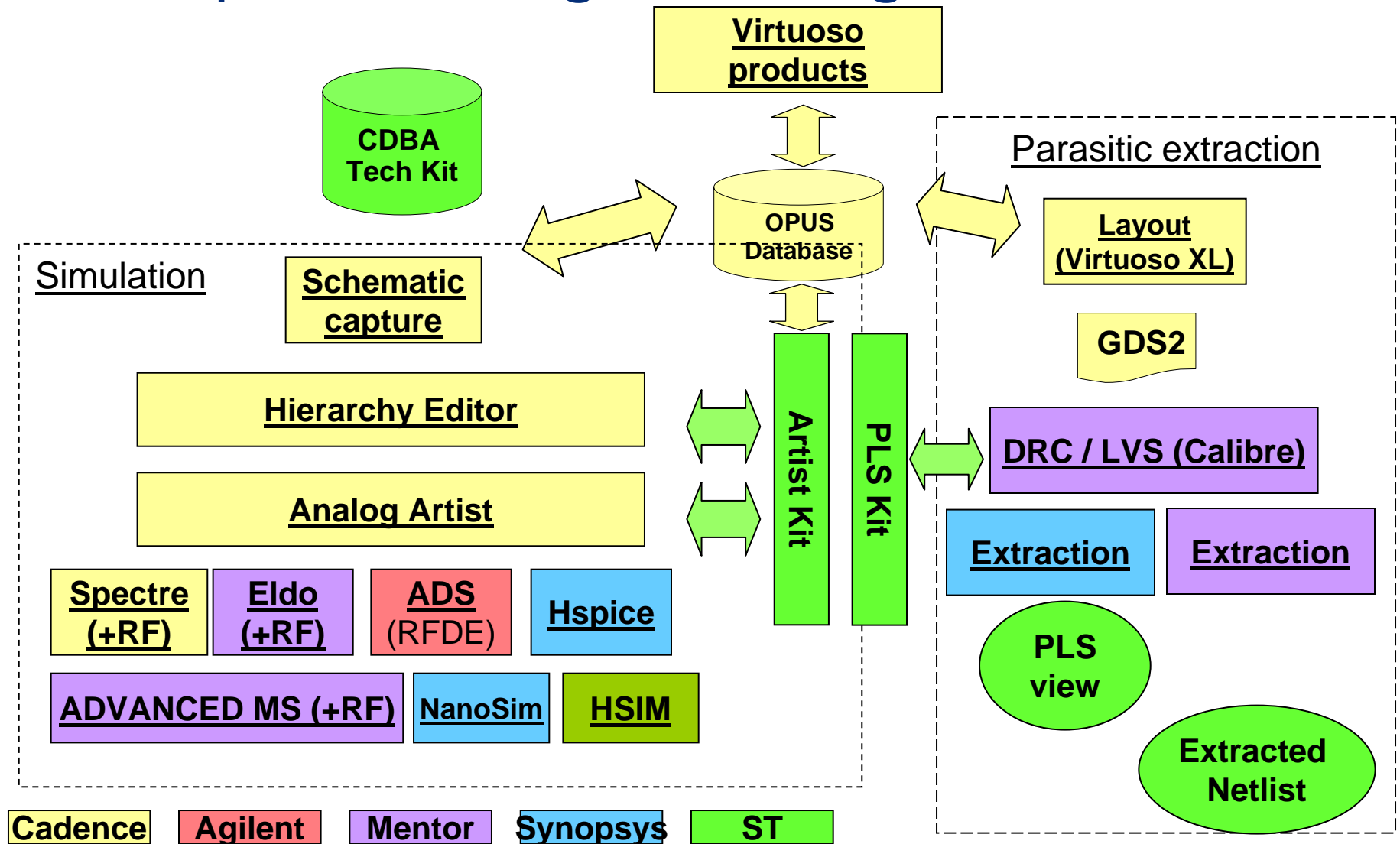
Status/Directions



FTM – Central CAD
& Design Solutions

Philippe
MAGARSHACK

«simple» Analog/RF design environment



Multiple design teams

IP blocks may come from several different groups or companies, with different CAD flows



Agilent Technologies
Innovating the HP Way

Today:



Plus many
resources

Analog Design Data Standards...

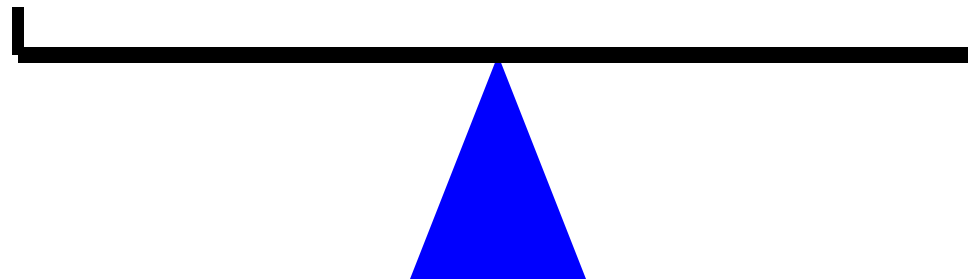
- 📄 Digital has standards : LEF/DEF/SDF/...
- 📄 Analog has had standards too : Spice/Spice/Spice

Analog EDA vendors have to deal with 'proprietary' constraints (CDBA)

→ innovation ↘

- Digital is becoming analog but analog CAD is not as efficient as Digital ;
- RF-SOC and RF-SIP = clear trend

→ need for innovation ↗



Physical Design kit standardization !

- ❏ Same information duplicated in incompatible tech files :
 - ❏ Vias, Enclosure rules, GDSII layers, metal stack
 - ❏ Even for a single vendor flow
- ❏ Each single tool has its own format 😞

Open Access is one STEP but many more are needed to reach the goal



Analog is not digital ...

- ▣ Analog Design means **hierarchical schematic** and parameter passing
- ▣ Analog design means **very complex PCELLs** for Inductors, Capacitors, ...
- ▣ Each vendor's implementation has a different solution in OA for these 2 issues:
 - ▣ Today we cannot exchange a real analog design from Vendor M OA to Vendor C OA without a lot of semi-automated processing

Three development directions for SIP

Design Kit integration

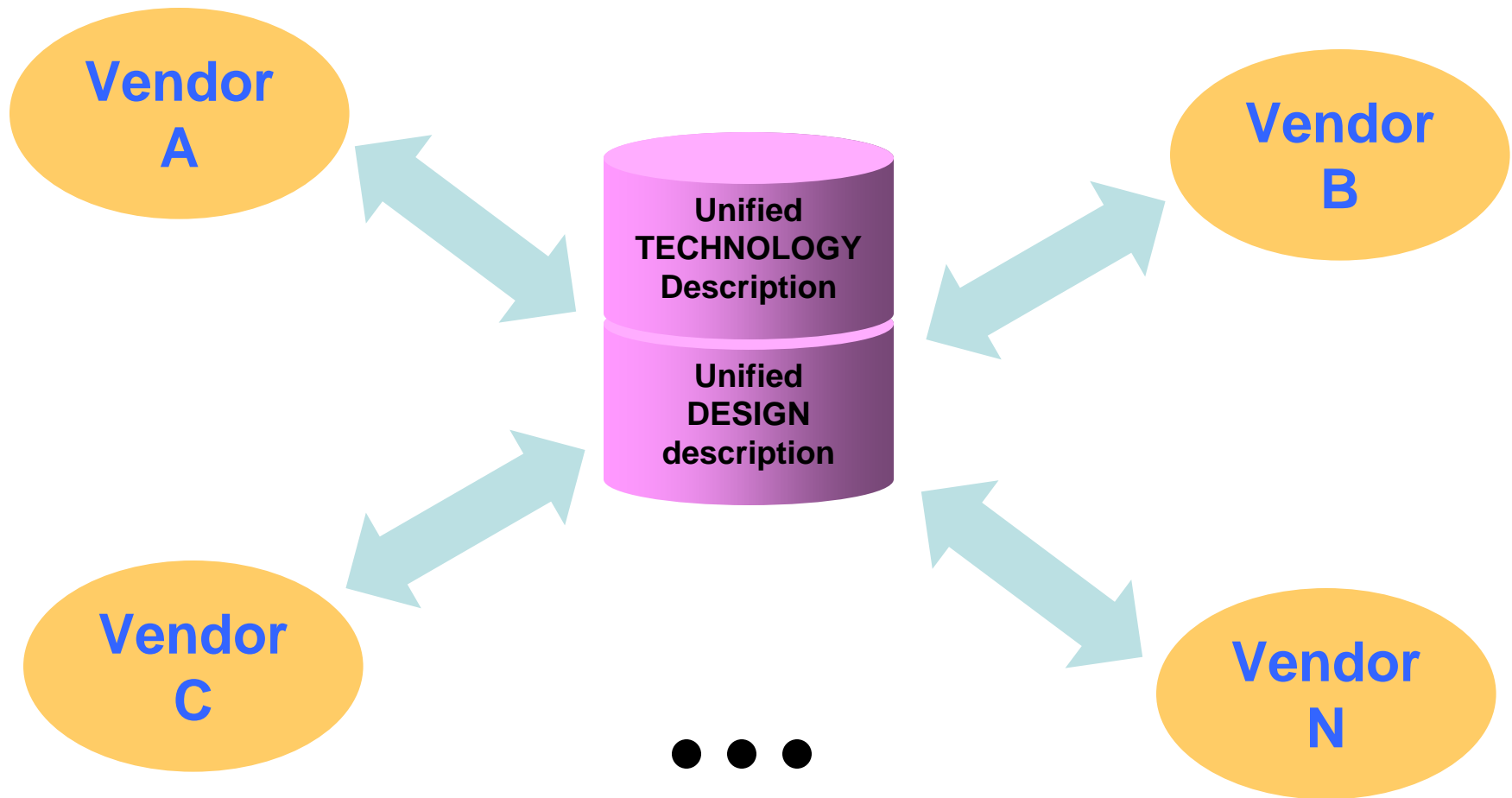
- DRM
- DRC
- Multi-environment
- LVS

Substrate Technology

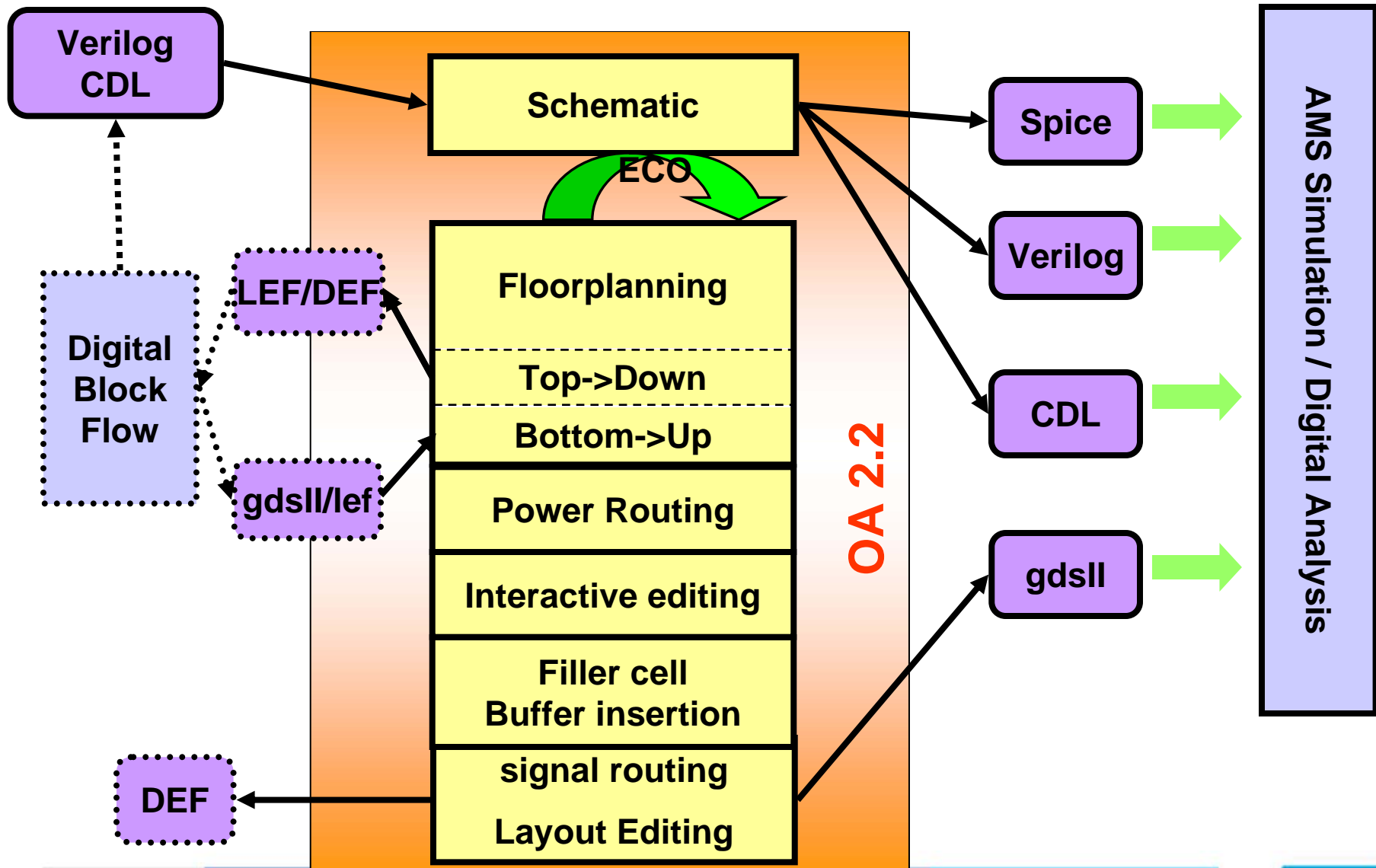
Emb passives design and modeling

- Define structures for 3D simulation
- Substrate modeling
- Electrical and geometrical measurements
- Generation of the equivalent lumped model

"The Dream"



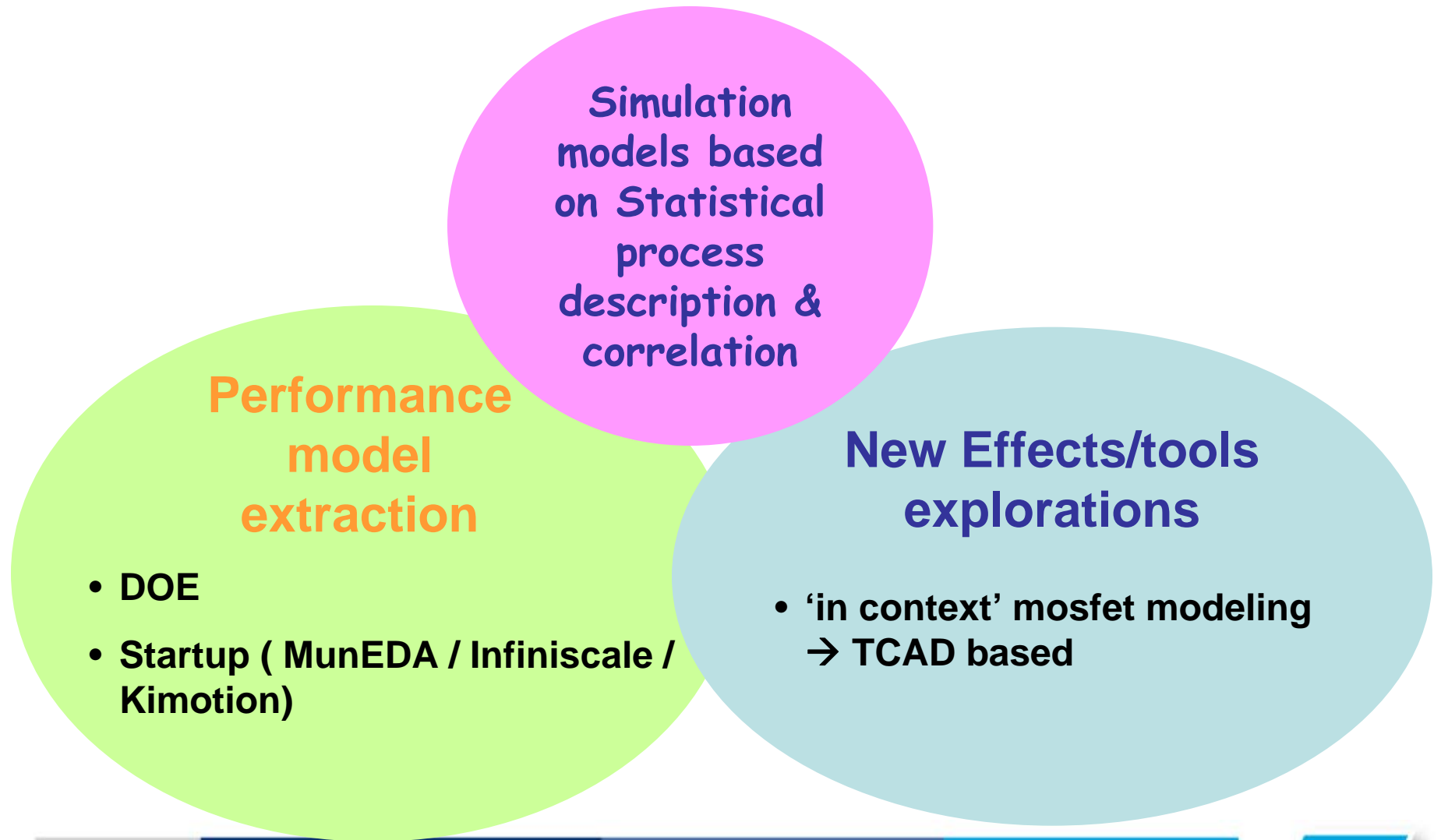
Analog On Top Flow for Digital/RF transceivers



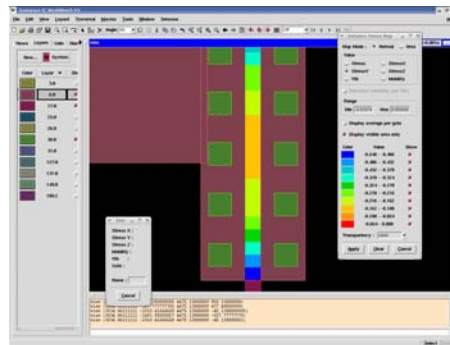
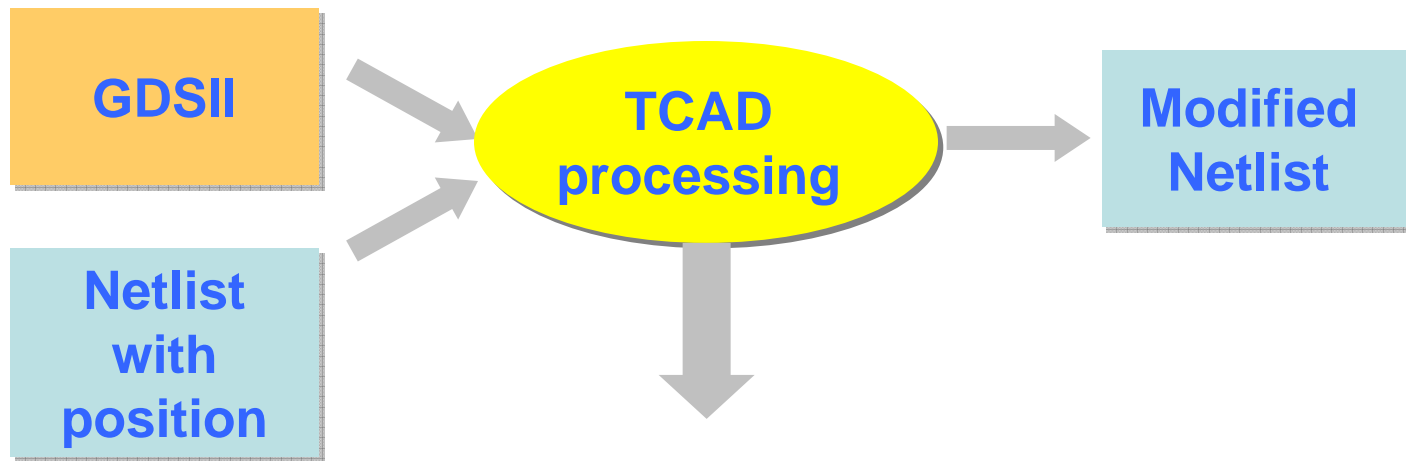


Standardize !

Process variability simulation @ transistor level for 65/45nm analog/RF

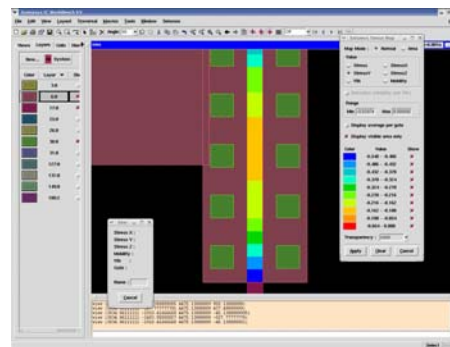
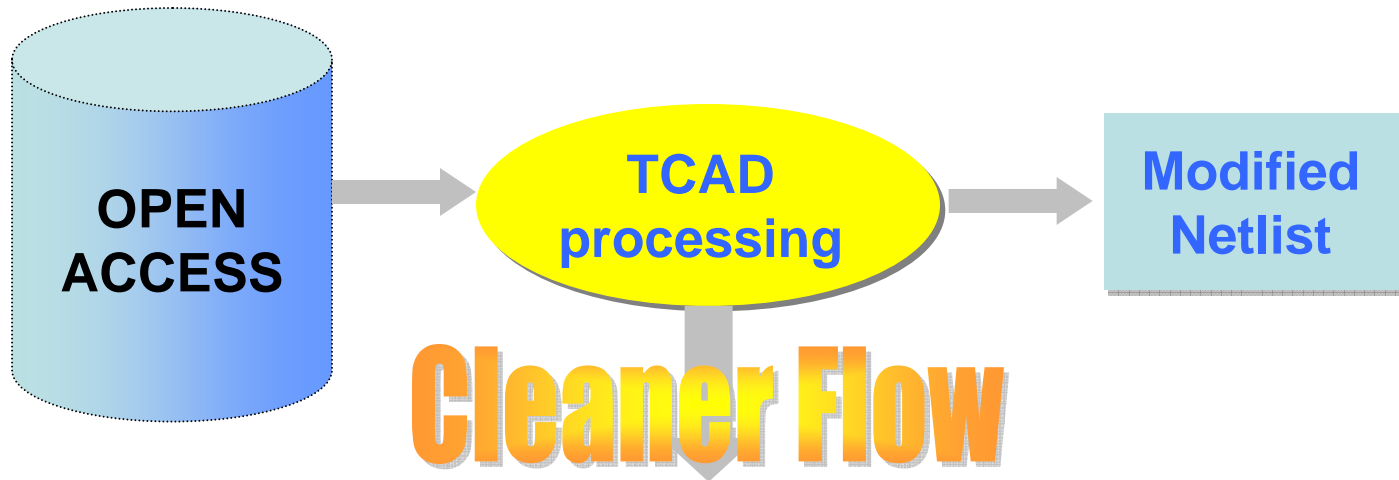


“In context” MOSFET simulation



Display
What if Analysis

“In context” MOSFET simulation



Display
What if Analysis

Conclusions

- Analog/RF EDA needs a database standard
 - OA a good first step

- But, missing:
 - Process-related information standard
 - P-CELL standard infrastructure

- To allow true design interchange, including simulation/test benches

Conclusions

- EDA innovation needed, to raise analog designers productivity:
- Design verification
- Design re-sizing
- Design layout optimization
- ... Architecture selection ???
- Analog/Dig/RF trade-offs, co-design
- Not only on SoC but SIP level
- ...

THANK YOU



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