

Wake Up to Wireless!

Enabling Complex Designs with Advanced Libraries and IP

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Interoperability Showcase
while enjoying breakfast

 Your Interoperability Partner

Wake Up to Wireless!

Enabling Complex Designs with Advanced Libraries and IP

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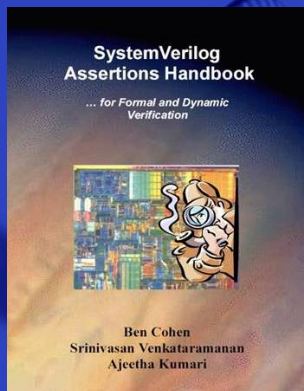
Dr. Chi-Foon Chan
President and
Chief Operating Officer
Synopsys

 Your Interoperability Partner

Program Highlights

SYNOPSYS®

- Wake up to the realities of SPIRIT IP and Composite Current Source (CCS) libraries that enable complex design
- Presentation of the 5th Tenzing Norgay Interoperability Achievement Award



- Drawings:
 - Sony® PSP™
 - IEEE EDA VuSpec™
 - SystemVerilog Assertions Handbooks

- Showcase open again after the program

➤ Your Interoperability Partner



Wake Up to SystemVerilog!

Unified Design and Verification Language Increases Engineering Productivity

- Visit the Accellera booth (#2284 near Hall D Food Court)
 - Synopsys' SystemVerilog solutions demo
 - Meet Synopsys and other SystemVerilog experts
- Attend the Doulos/Synopsys "Assertion-Based Verification with SystemVerilog" workshop
 - Thursday, 11:30AM-2:00PM, Room 202A, Convention Center
- Visit Synopsys booth (#1088)
 - SystemVerilog product updates and demos
- Start using SystemVerilog today!

 Your Interoperability Partner

Wake Up to the IEEE-SA!

- IEEE recognizes the need for *fast, market-relevant* standards
- IEEE P1800 SystemVerilog standardization progress
 - DAC 2004: Transferred from Accellera to IEEE-SA
 - DAC 2005: In the ballot process
- IEEE Corporate Standards Program
 - Utilizes procedures that allow working groups to begin technical work immediately
 - Provides level playing field – “One company, One vote”
 - Offers experienced professional staff to expedite process
 - Leverages existing liaisons to international standardization (IEC/IEEE dual logo)



IEEE

IEEE Standards Association

Corporate Members at DAC 2005

The image displays a grid of logos for various corporate members of the IEEE Standards Association at the DAC 2005 conference. The logos are arranged in approximately 10 rows and 10 columns. The members include:

- Row 1:** Mitra (An AGFA Company), CEA (Canadian Electricity Association - The voice of Canadian electricity), THERMON, GBT, accellera, Infineon technologies, SBC.
- Row 2:** M-Systems (Flash Disk Pioneers), DISA, SYNOPSYS, AEROTEK, S² Technologies (Storage and Server I/O Solutions), Rotani Inc., IBM.
- Row 3:** net₂ (Net-O₂ Technologies), bluespec, ARM, FINTRONIC, USA, Satyam (What Business Demands), SANYO.
- Row 4:** BROADCOM, Deutsch Advanced Interconnect, HART (INTEGRATED), Lucent Technologies (Bell Labs Intellectual), Sun microsystems, Mentor Graphics.
- Row 5:** intel, CALYPTO, Sutherland HDL, Inc., Synplicity (Simply Better Results), JEITA.
- Row 6:** WildPackets, SOLARFLARE Communications, Allied Telesis, Pacific Broadband Networks, JASPER (design automation).
- Row 7:** NORTEL NETWORKS (BUSINESS WITHOUT BOUNDARIES), Kingston TECHNOLOGY, SIEMENS, hp, MARYLAND PROCUREMENT OFFICE, ALTERA.
- Row 8:** Sunburst Design, SONY, GO Networks, invent, Deutsche Telekom, Sprint, NOKIA.
- Row 9:** AirFLOW NETWORKS, verizon wireless (We never stop working for you.®), Volex, MOTOROLA (intelligence everywhere), JEDA Technologies, cadence.
- Row 10:** King Abdul Aziz University, SOLECTRON, IEEE-ISTO, Flarion, Saudi Aramco.

Wake Up to Interoperability!

- Look at your EDA and IP suppliers today
 - Standardizing on formats and languages to meet your needs
- EDA vendors cooperating to resolve tool interoperability issues



Wake Up to Interoperability!

June 06, 2005 08:03 AM US Eastern Timezone

The Open SystemC Initiative Announces Availability of the SystemC Transaction-level Modeling Standard with Broad Industry Support

SAN JOSE, Calif.--(BUSINESS WIRE)--June 6, 2005--The Open SystemC Initiative (OSCI) today announced the delivery of the SystemC(TM) Transaction-level Modeling (TLM) Standard 1.0. The availability of a standard SystemC TLM library promotes industry-wide re-use of transaction-level Intellectual Property (IP) and the development of tools to provide a rich design environment for transaction-level design and verification.

The new TLM standard defines application programming interfaces (APIs) and provides a foundation layer upon which interoperable transaction-level communication can be built. The standard library implementation can be downloaded under the open source license at www.systemc.org.

Design at the transaction-level enables users to efficiently develop system-level models, assist in architecture analysis and enable early software development, benefit from high-level simulation, transaction-level IP models are also ideal golden reference models that can be used in testbenches and simulation environments, maximizing investments in high-level models. In addition, the standard provides simulation performance more than 100 fold making it possible to meaningfully validate system-level models. Simulation speeds are also required for the validation of IP in the context of the system-level design. The standard provides abstraction levels from algorithm to TLM and RTL makes it the ideal framework for system-level design and validation.

"The SystemC TLM 1.0 kit was announced by the OSCI Working Group and Board for public release on the SystemC website," said Mark Harris, OSCI Working Group chair. Harris added to note that today it is in use at major companies, with the intent to use it in a wide range of system-level designs.

"More than 50 semiconductor companies have participated in the development and review of the standard APIs and open source implementation of the SystemC TLM foundation that enables the industry to widely adopt Transaction-Level Modeling (TLM) Standard 1.0," said Harris. Harris is also a member of the OSCI TLM Working Group chair.

"This standard is the result of a number of companies cooperating in the definition and necessary documentation. It is another step in enabling both system-level design and interoperability between companies to grow. Building on this standard, system-level simulation will take another step in becoming an accepted phase in the development of complex SoC system designs," said Ralph von Vignau, an OSCI Board member.

With this new standard being met with support from a broad range of semiconductor companies and EDA suppliers, users have a wide choice in vendors supporting this flow. Companies and organizations endorsing this standard include Cadence Design Systems, CoWare, Forte Design Systems, Mentor Graphics, Royal Philips Electronics, STMicroelectronics, Synopsys, Inc., Atrenta, Inc., Calypto Design Systems, Inc., Celoxica Ltd, ChipVision Design Automation AG, Synfora, Inc., Summit Design Automation, Inc and OCP-IP.

To download an open source license of the new TLM standard and library implementation visit www.systemc.org.

SystemC Specification for Transaction-level Models

today

needs to meet your

the tool

our Interoperability Partner

Wake Up to Interoperability!

June 06, 2005 08:03 AM US Eastern Timezone

The Open SystemC Initiative Announces Availability of the SystemC Transaction-level

Mode

Synopsys Joins Si2

SAN JOSE, Calif. (June 6, 2005) — The SystemC Initiative (Si2) today announced the availability of the SystemC Transaction-level Modeling (TLM) architecture, which will promote interoperability between design tools.

The new TLM architecture is a key component of the SystemC Initiative's vision of a unified design flow for the implementation of complex systems-on-chips (SoCs).

Design tools that support the TLM architecture will be able to maximize productivity and reduce time-to-market for the development of SoCs. TLM architecture is a key component of the SystemC Initiative's vision of a unified design flow for the implementation of complex systems-on-chips (SoCs).

"The SystemC Initiative is pleased to announce the addition of Synopsys to the TLM architecture. Synopsys' leadership in the design automation industry is a welcome addition to Si2 and will help us to better address the design flow and modeling needs."

"More than 100 design automation vendors and customers alike can work together to solve shared challenges that are critical to the growth of the industry," said Steven E. Schulz, President and CEO of Si2. "Synopsys' leadership in the design automation industry is a welcome addition to Si2 and will help us to better address the design flow and modeling needs."

"This step is a key component of the SystemC Initiative's vision of a unified design flow for the implementation of complex systems-on-chips (SoCs). Synopsys' leadership in the design automation industry is a welcome addition to Si2 and will help us to better address the design flow and modeling needs."

With this announcement, Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has

To download the SystemC Initiative TLM architecture, visit www.systemcinitiative.org.

DESIGN AUTOMATION CONFERENCE, ANAHEIM, CA, June 14, 2005 – Synopsys, Inc. (Nasdaq:SNPS), a world leader in semiconductor design software, today announced it is joining Si2 as a result of the company's increased presence in analog simulation. As a member of Si2, Synopsys will advocate the migration of analog design to SystemC. Synopsys is also making available to Si2 its open source Liberty™ CCS model.

"It is the mark of a healthy industry when competitors and customers alike can work together to solve shared challenges that are critical to the growth of the industry," said Steven E. Schulz, President and CEO of Si2. "Synopsys' leadership in the design automation industry is a welcome addition to Si2 and will help us to better address the design flow and modeling needs."

"Joining Si2 at this juncture is a key component of Synopsys' continued push to offer end users the best design solutions," said Rich Goldman, vice president, Strategic Market Development, Synopsys. "Synopsys has been making significant strides to serve the entire electronic design community. As a member of Si2, Synopsys is now working with Si2 to determine the significant role it will play in the standards organization."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has

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June 06, 2005 08:03 AM US Eastern Timezone

The Open SystemC Initiative Announces Availability of the SystemC Transaction-level

Mode

Synopsys Joins Si2

SAN JOSE, Calif. (BUSINESS WIRE)--June 6, 2005--PDF Solutions® (Nasdaq:PDFS - News) and Synopsys, Inc. (Nasdaq:SNPS - News) today announced that they have entered into a strategic partnership to promote interoperability between their design tools and manufacturing processes.

The new layer up implementation will enable designers to maximize their productivity and reduce time-to-market for the next generation of TLM and SystemC designs.

Design architects can now maximize their productivity and reduce time-to-market for the next generation of TLM and SystemC designs.

"The SystemC design methodology is a key enabler for the next generation of TLM and SystemC designs."

"More than 100 leading semiconductor companies are now using the SystemC design methodology to accelerate their time-to-market for the next generation of TLM and SystemC designs."

"This step in the evolution of the SystemC design methodology is a key enabler for the next generation of TLM and SystemC designs."

With this new partnership, Synopsys and PDF Solutions are providing the top-of-the-line infrastructure necessary for considering the cell selection process."

To download the SystemC design methodology, visit www.pdf.com

DESIGN (Nasdaq:PDFS - News) and Synopsys, Inc. (Nasdaq:SNPS - News) today announced that they have entered into a strategic partnership to promote interoperability between their design tools and manufacturing processes.

"Joining the best of both worlds, PDF Solutions' yield models and Synopsys' Liberty library format for cell-based yield modeling, PDF Solutions' .pdfm format and pDfx(TM) process-aware design for manufacturability (DFM) environment, and Synopsys' Galaxy(TM) IC Compiler, the next generation of yield data through Liberty library format, letting Synopsys and PDF Solutions' mutual customers benefit from faster time-to-market, increased IC yield and performance, and improved product reliability and profitability. Headquartered in San Jose, Calif., PDF Solutions operates worldwide. For more information, visit www.pdf.com

About Synopsys, Inc. Synopsys, Inc. is a leading provider of process-design integration technologies to enhance IC manufacturability. PDF Solutions' software, methodologies, and services enable semiconductor companies to create IC designs that are more manufacturable, and manufacturing processes that are more capable. By simulating nanometer-scale product and process interactions, PDF Solutions offers customers faster time-to-market, increased IC yield and performance, and improved product reliability and profitability. Headquartered in San Jose, Calif., PDF Solutions operates worldwide. For more information, visit www.pdf.com

PDF Solutions and Synopsys Extend Liberty Library Format for Yield Optimization with IC Compiler

Tuesday June 7, 11:00 am ET

Delivering Faster Time-to-Results and Better Quality-of-Results for Yield-Driven Optimizations

SAN JOSE, Calif.--(BUSINESS WIRE)--June 7, 2005--PDF Solutions®, Inc. (Nasdaq:PDFS - News) and Synopsys, Inc. (Nasdaq:SNPS - News) today announced that they have entered into a strategic partnership to promote interoperability between their design tools and manufacturing processes. The two companies are working together to achieve a new level of designer productivity for yield optimization. The two companies have entered into a strategic partnership to promote interoperability between their design tools and manufacturing processes. The two companies are working together to achieve a new level of designer productivity for yield optimization. The two companies have entered into a strategic partnership to promote interoperability between their design tools and manufacturing processes. The two companies are working together to achieve a new level of designer productivity for yield optimization.

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"The combination of PDF Solutions' yield models with the Synopsys Liberty library format for cell-based yield modeling, PDF Solutions' .pdfm format and pDfx(TM) process-aware design for manufacturability (DFM) environment, and Synopsys' Galaxy(TM) IC Compiler, the next generation of yield data through Liberty library format, letting Synopsys and PDF Solutions' mutual customers benefit from faster time-to-market, increased IC yield and performance, and improved product reliability and profitability. Headquartered in San Jose, Calif., PDF Solutions operates worldwide. For more information, visit www.pdf.com

"It is the combination of PDF Solutions' yield models with the Synopsys Liberty library format for cell-based yield modeling, PDF Solutions' .pdfm format and pDfx(TM) process-aware design for manufacturability (DFM) environment, and Synopsys' Galaxy(TM) IC Compiler, the next generation of yield data through Liberty library format, letting Synopsys and PDF Solutions' mutual customers benefit from faster time-to-market, increased IC yield and performance, and improved product reliability and profitability. Headquartered in San Jose, Calif., PDF Solutions operates worldwide. For more information, visit www.pdf.com

At 90 nm and below, interactions between the product and process are becoming increasingly complex. Designers must increasingly consider yield as a cost function that must be optimized during the routing stage by applying special techniques. PDF Solutions is extending Liberty library format for cell-based yield modeling, PDF Solutions' .pdfm format and pDfx(TM) process-aware design for manufacturability (DFM) environment, and Synopsys' Galaxy(TM) IC Compiler, the next generation of yield data through Liberty library format, letting Synopsys and PDF Solutions' mutual customers benefit from faster time-to-market, increased IC yield and performance, and improved product reliability and profitability. Headquartered in San Jose, Calif., PDF Solutions operates worldwide. For more information, visit www.pdf.com

Designers must increasingly consider yield as a cost function that must be optimized during the routing stage by applying special techniques. PDF Solutions is extending Liberty library format for cell-based yield modeling, PDF Solutions' .pdfm format and pDfx(TM) process-aware design for manufacturability (DFM) environment, and Synopsys' Galaxy(TM) IC Compiler, the next generation of yield data through Liberty library format, letting Synopsys and PDF Solutions' mutual customers benefit from faster time-to-market, increased IC yield and performance, and improved product reliability and profitability. Headquartered in San Jose, Calif., PDF Solutions operates worldwide. For more information, visit www.pdf.com

"Our leading-edge, top-of-the-line interconnect yield optimizations provided in our routing technology," said Saleem Haider, senior director of physical synthesis, PDF Solutions. "Working with PDF Solutions, we are now expanding this support into our cell selection process."

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About PDF Solutions

PDF Solutions, Inc. (Nasdaq:PDFS - News) is the leading provider of process-design integration technologies to enhance IC manufacturability. PDF Solutions' software, methodologies, and services enable semiconductor companies to create IC designs that are more manufacturable, and manufacturing processes that are more capable. By simulating nanometer-scale product and process interactions, PDF Solutions offers customers faster time-to-market, increased IC yield and performance, and improved product reliability and profitability. Headquartered in San Jose, Calif., PDF Solutions operates worldwide. For more information, visit www.pdf.com

Liberty Extensions for Yield Optimization

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Wake Up to Interoperability!

June 06, 2005 08:03 AM US Eastern Timezone

The Open SystemC Initiative Announces Availability of the SystemC Transaction-level Model

SAN JOSE, Calif. – Synopsys, Inc. today announced the SystemC Transaction-level Model (TLM) is now available for download.

The new TLM layer up to the implementation of the design models, maximizing the TLM and CE addition.

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PDF Solutions and Synopsys Extend Liberty Library Format for Yield Optimization with IC Compiler

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Synopsys Announces Industry-Wide Support For Liberty™ Composite Current Source (CCS) Library Models

ARM, TSMC, Virage Logic and Library Technologies Gear Up Libraries

Enabled 90nm

MOUNTAIN VIEW, Calif., June 14, 2005 – Synopsys, a leading semiconductor design software, today announced that ARM, TSMC, Virage Logic and Library Technologies support of Synopsys Composite Current Source (CCS) models in their intellectual property (IP) for accurate current source calculation to within two percent, reducing design accuracy delay and time to results with improved design quality of results

"ARM's long-standing mutual customer, Synopsys, focuses on making available to our customers the Liberty Composite Current Source (CCS) models. Neal Carney, vice president of Marketing, said, "Synopsys' support of its products supporting a large number of customers has enhanced its characterization infrastructure to generate Liberty CCS models enable higher accuracy and more efficient voltage scaling capabilities in scaled process demands and new design styles, like the ARM® Intelligent Energy Management technology. CCS models for the ARM Artisan® SAGE-X™ standard cell library on TSMC's 90-nanometer GT process are immediately available for download to beta customers."

Industry-Wide Support for Liberty CCS Library Models

ay

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Partner

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June 06, 2005 08:03 AM US Eastern Timezone

The Open SystemC Initiative Announces Availability of the SystemC Transaction-level Model

SAN JOSE, Calif. (June 6, 2005) — The SystemC Initiative promotes design interoperability.

The new layer up implementation

Design architectures, models, and data are maximized for the VLSI and TLM and

"The SystemC Initiative with the

"More than 100 and open Level Model

"This step in simulation and synthesis

With this Design Inc., At Design

To download

Synopsys Joins Si2

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Synopsys Announces Industry-Wide Support For Liberty™ Composite Current Source (CCS) Library Models

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SPIRIT Consortium – SPIRIT 1.0 Public Release

Release of SPIRIT specification enables IP interoperability

December 8, 2004

The SPIRIT (Structure for Packaging, Integrating and Reusing Intellectual Property) Consortium, a group of leading companies in the field of IP creation, has announced the release of the approved SPIRIT specification. Today's (System-on-Chip) designers worldwide can now use that will enable them to select, configure and integrate different SPIRIT-compatible components using a range of different SPIRIT-compatible tools.

The persistent goal of the SPIRIT Consortium is to streamline the system integration process has been plagued by the a variety of IP integration and configuration. Consequently, many or labor-intensive, hindering adoption. By allowing IP integration and configuration in a standard XML format, the SPIRIT specification provides the vital link that will allow components to flow seamlessly into multiple tool flows. The standardization will give designers the benefits of a richer IP pool coupled with a wider choice of design environments. SPIRIT provides a real competitive edge to IP providers and tool vendors that adopt the standard. IP vendors will benefit from a standardized way of making their deliverables compatible with customer design flows, and tool vendors will have a large pool of IP that can be automatically imported, configured and integrated using their design tools.

SPIRIT for IP Packaging & Reuse v1.1 Released at DAC 2005

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Wake Up to SPIRIT!

- How do you combine IP from various sources quickly and efficiently?
- Industry-level cooperation is needed
 - Define IP description standards
 - Enable tools that raise automation levels and cut costs
- Improving ease-of-use and increasing flexibility in IP selection and integration.





SPIRITed speakers:

- John Swanson, Synopsys
- Chris Lennard, ARM

See SPIRIT in action!

- ***Stop by the SPIRIT Showcase***
- ***Visit the ARM and Synopsys booths
(#1309 and #1379 in Hall C)***

 Your Interoperability Partner

Wake Up on Mt. Everest!

- More opportunities to summit
 - More understanding, infrastructure, tools, and technology advancements
 - More climbers are successful
- Same true in interoperability
 - More companies participating
 - More technology donations
 - More well-defined processes
- Therefore, designers are more successful



© Eurocopter

Rumor: Helicopter landed on Mt. Everest on May 14, 2005

5th Annual Tenzing Norgay Interoperability Achievement Award



- Presented to a company that
 - Surpasses common levels of interoperability
 - Contributes to overall industry advancement
 - Provides a new view of the future
 - Ensures customer success

 *Your Interoperability Partner*

■ Previous Award Winners

- CoWare (2001)
- Mentor Graphics (2002)
- Silicon Metrics (2003)
- Novas Software (2004)



■ 2005 Nominees

- @HDL
- ARM
- Atrenta
- Electronic Tools Company
- Library Technologies
- Verific Design Automation
- Zenasis

And the winner is...



ARM®



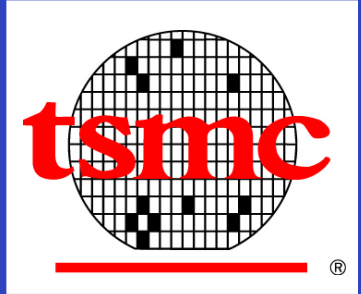
 *Your Interoperability Partner*

Wake Up to Current Based Modeling!

Next Generation Modeling for Timing, Noise, Power & Variation

- 1st order nanometer effects impact QoR
 - Miller capacitance, high impedance nets, dynamic IR-drop
 - Lead to higher library and design margins
- Liberty™ Composite Current Source (CCS)
 - Best gate-level representation of transistor behavior
 - Full Galaxy™ Design Platform support

Announcing Industry-Wide Support for CCS



 *Your Interoperability Partner*

CCS Libraries speakers:

- Bill Mullen, Synopsys
- Rob Aitken, ARM
- Edward Wan, TSMC



Wake Up with the EDA industry!

- Adopt the SPIRIT standard now
- Demand Liberty CCS libraries and tool support
- Get involved! Participate in the standards process



Thank you!

SYNOPSYS®

Wake Up to Wireless!

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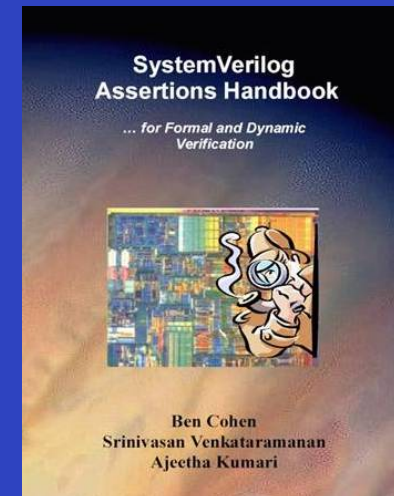
 **Your Interoperability Partner**

June 15, 2005

Wake Up to Prizes!

SYNOPSYS®

- Visit the Interoperability Showcase
- Talk with the panelists
- Turn in your feedback form to enter the drawing for a Sony PSP and *SystemVerilog Assertions Handbook*



- Drop your business card at the IEEE Showcase table to win your own copy of “EDA VueSpec”

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The Interoperability Showcase
will remain open until 10:00AM

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