

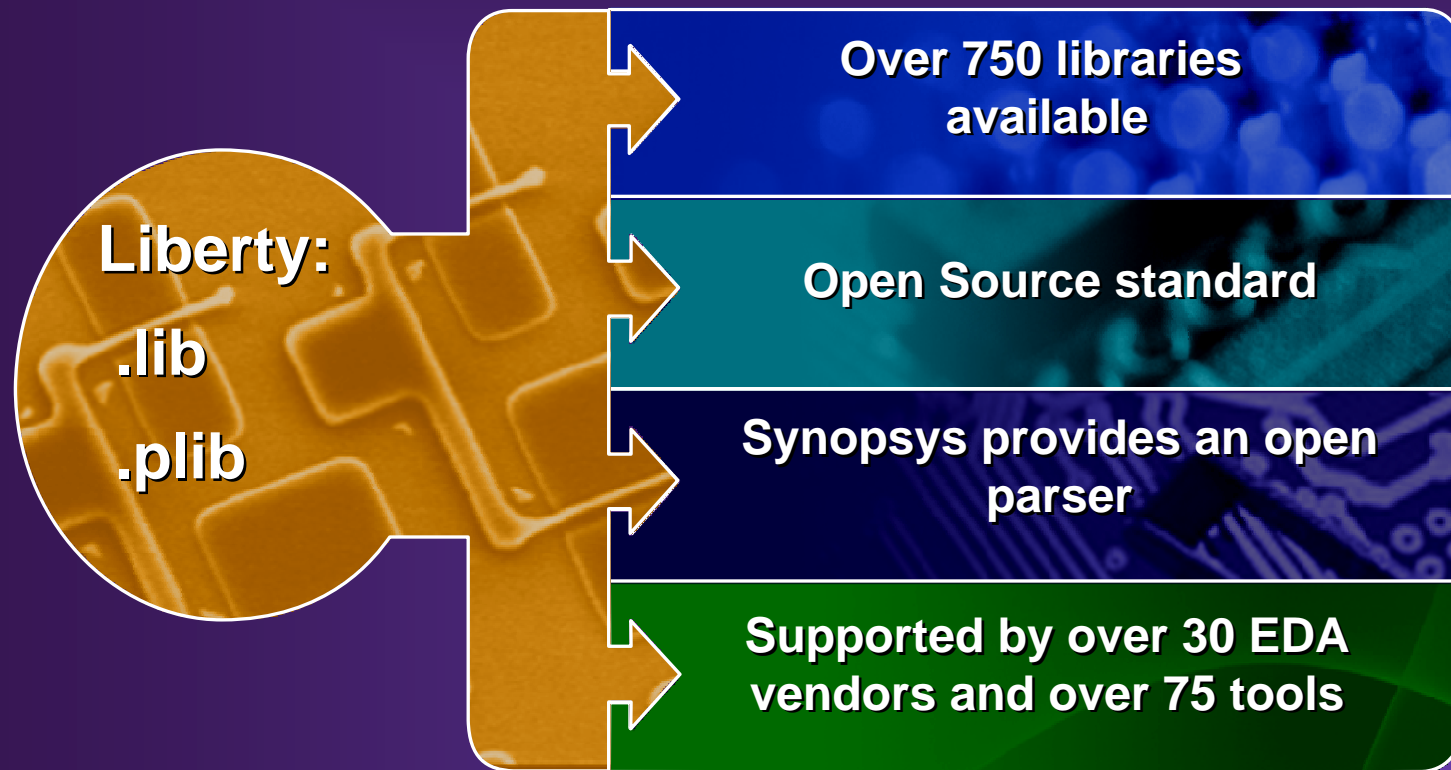
DAC'05

CCS-Timing: Composite Current Source Delay Modeling

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DAC 2005



Liberty™ Today – An Industry Standard



Liberty™ Today

Non-Linear Delay Models (NLDM)

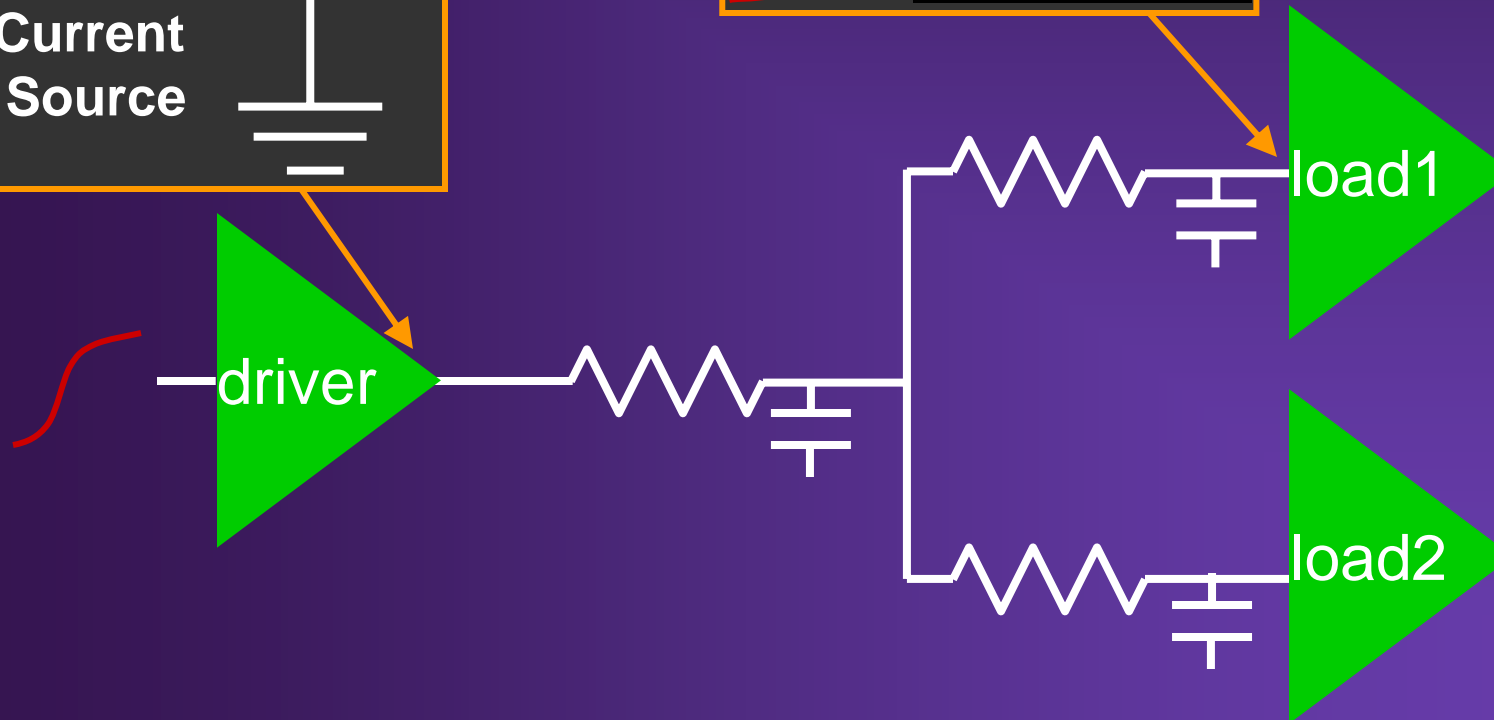
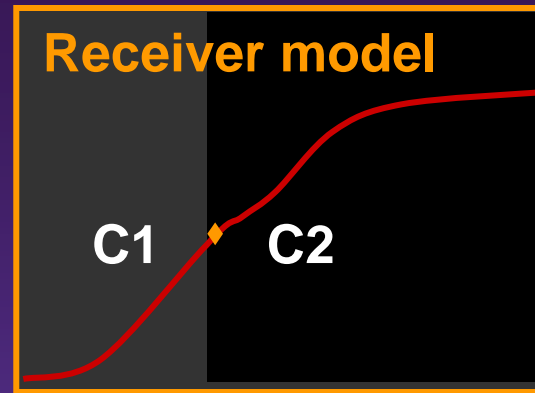
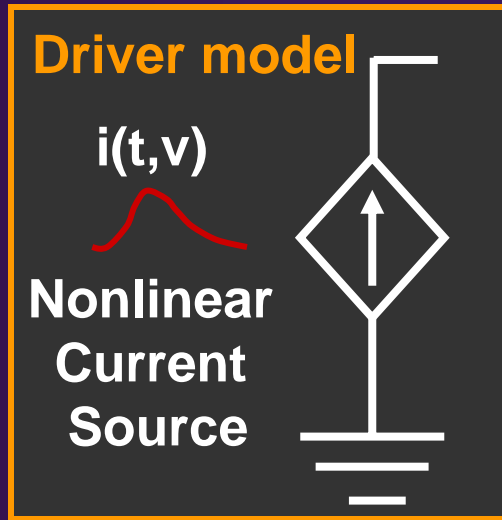
Timing

Noise

Power

- **Modeling challenges at 90-nm and below:**
 - High Impedance Interconnect
 - Miller Effect
 - Dynamic IR-Drop
 - Multi-Voltage
 - Temperature Inversion
 - Large # of cells
 - Increasing Variations

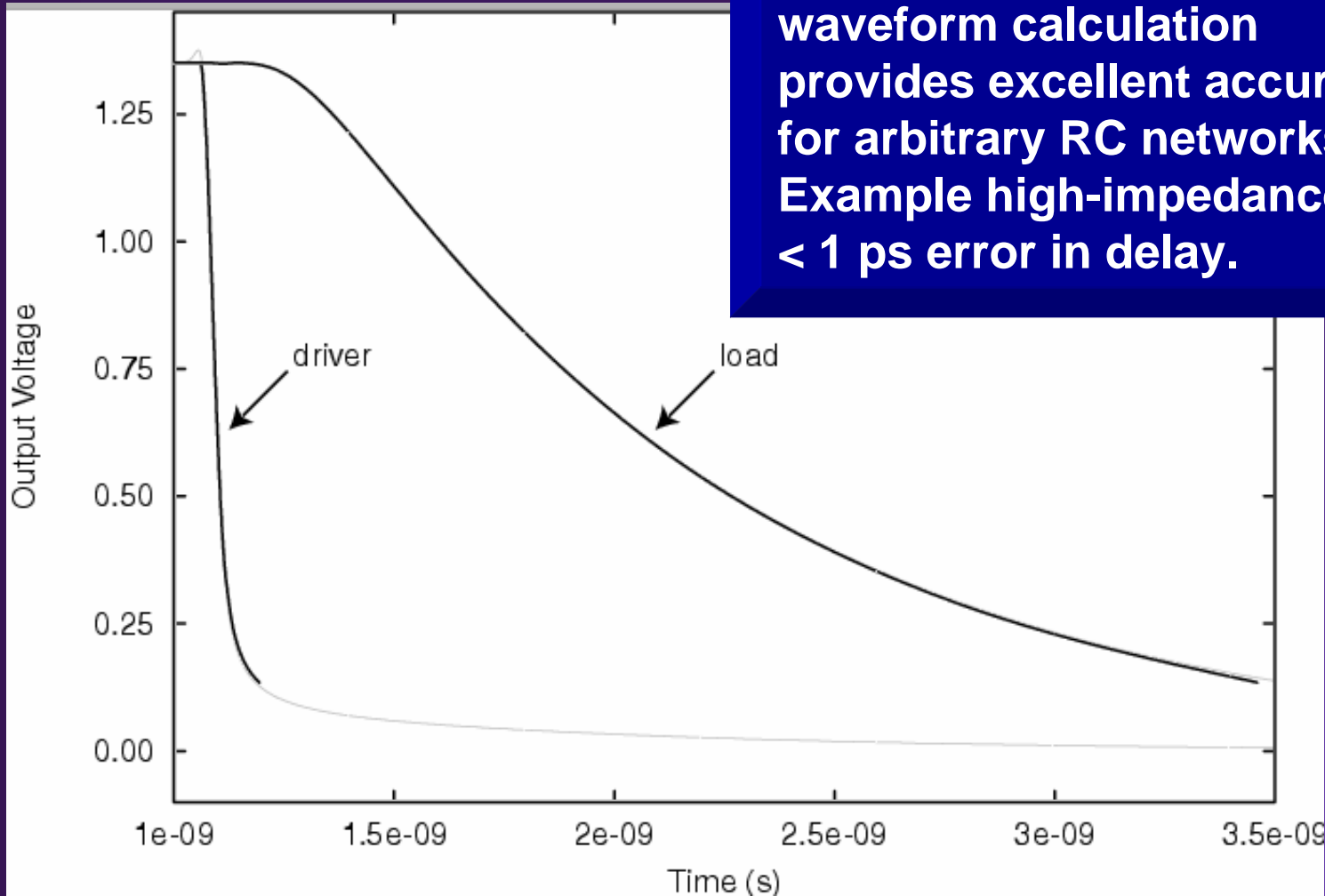
What is CCS-Timing?



CCS-Timing Benefits

Accuracy vs. HSPICE®

CCS-Timing current waveform calculation provides excellent accuracy for arbitrary RC networks. Example high-impedance net; < 1 ps error in delay.

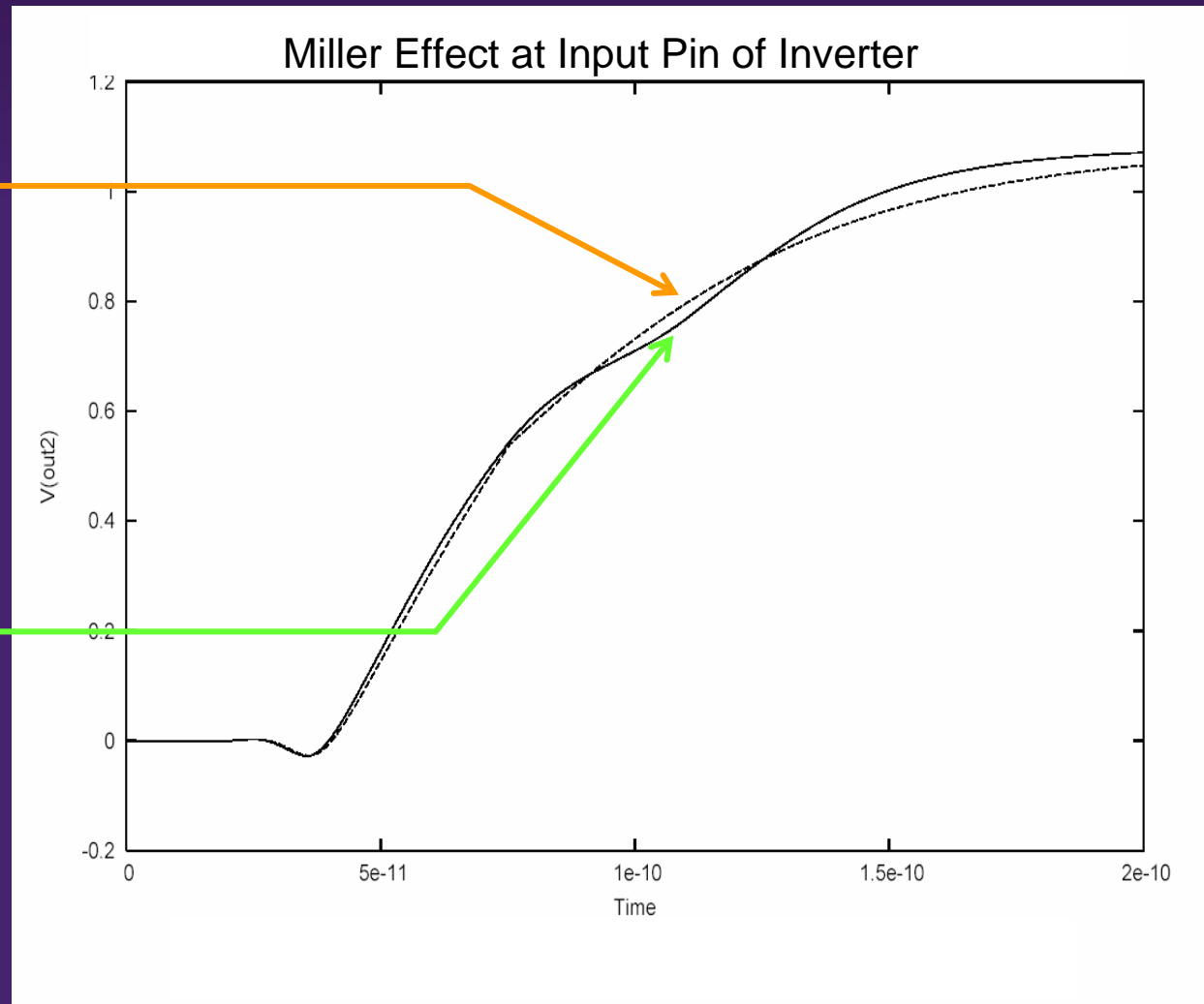


CCS-Timing Benefits

High-accuracy slew calculation

CCS Receiver Model results match delay and slew

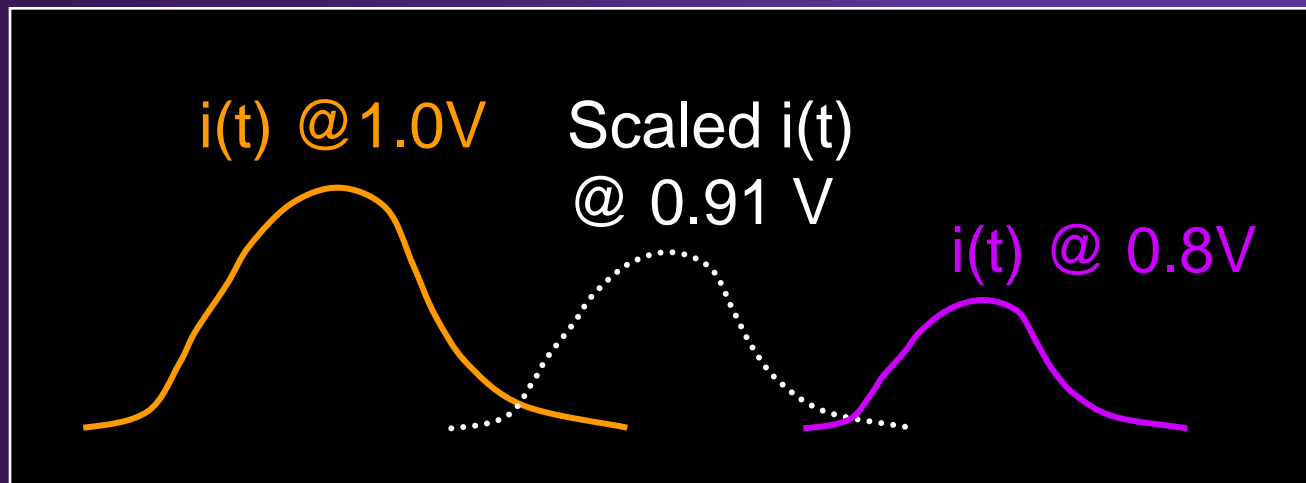
Miller effect at input pin of inverter



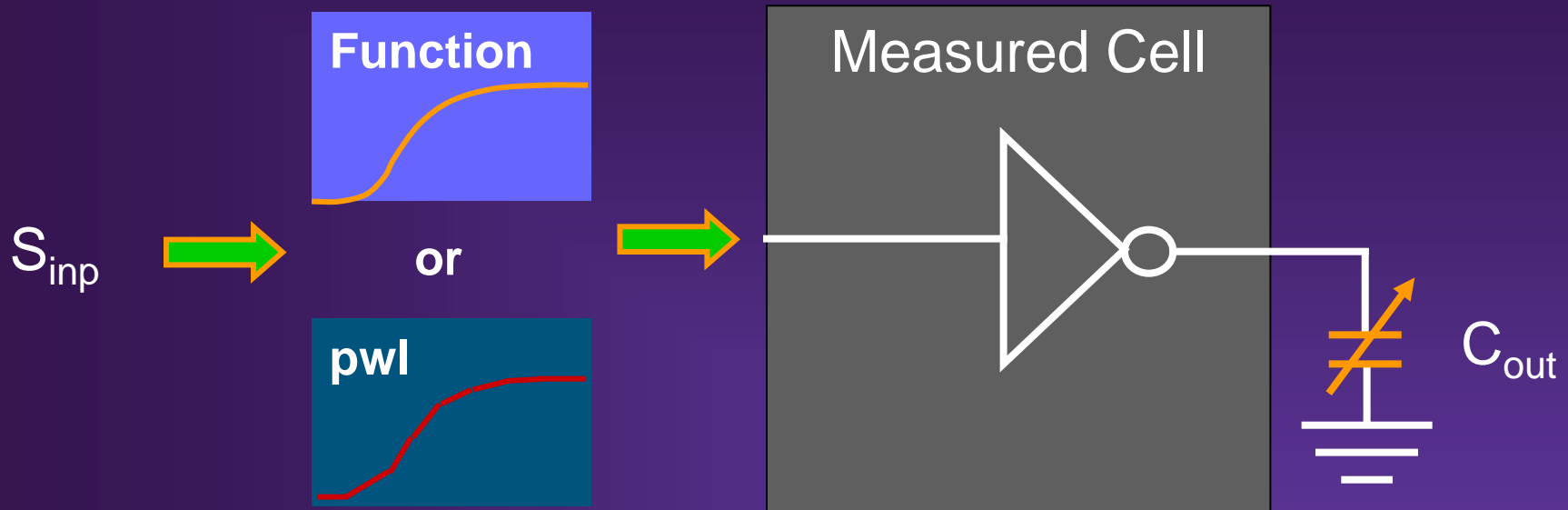
Benefits of CCS-Timing

Powerful scaling technology

- Nonlinear scaling of current waveform for highest accuracy
- Supports IR Drop, Multi- V_{dd} , and DVFS
- Also supports scaling of Temperature
- Proven extensibility for process variation: L_{eff} , V_{th} , ...



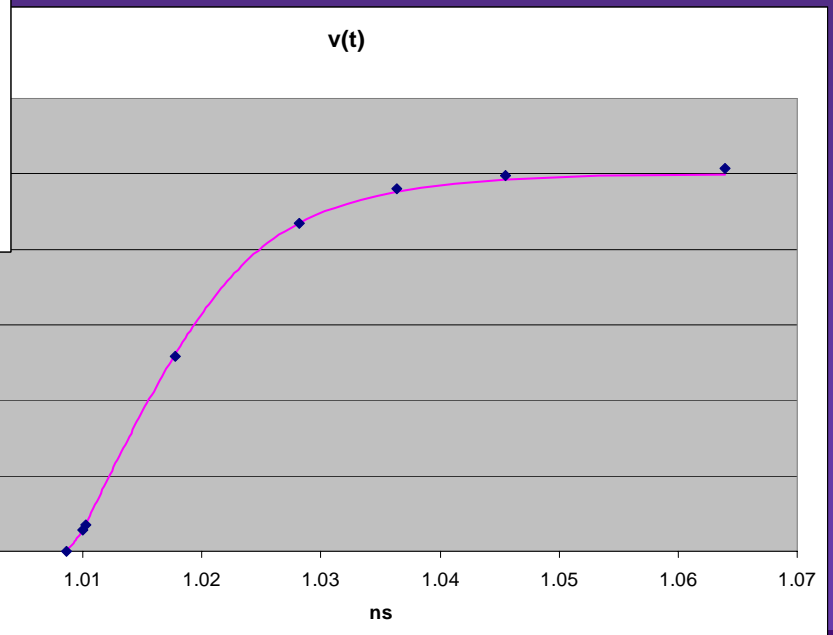
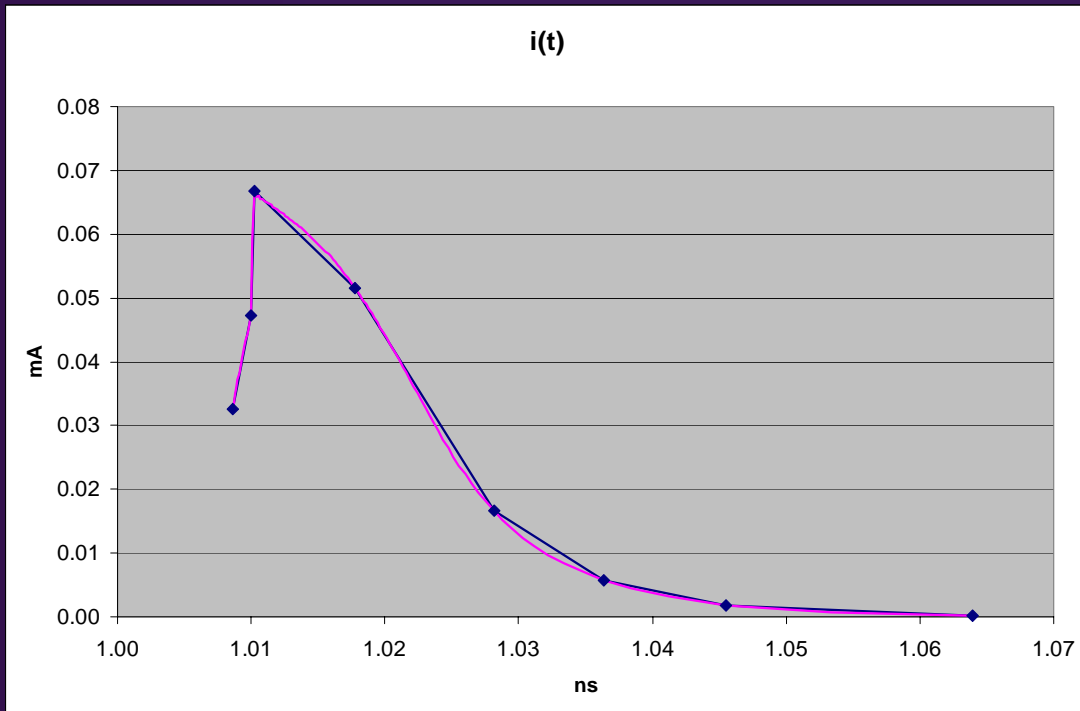
Characterization for CCS-Timing



- Apply a function or pwl that represents the desired input waveshape for each table index S_{inp} value
 - Choose a waveshape that is typical of real nets
- Measure current through C_{out} and into cell input
- Convert this data into compact driver / receiver model

CCS-Timing Driver Model Data

Efficient native current source representation



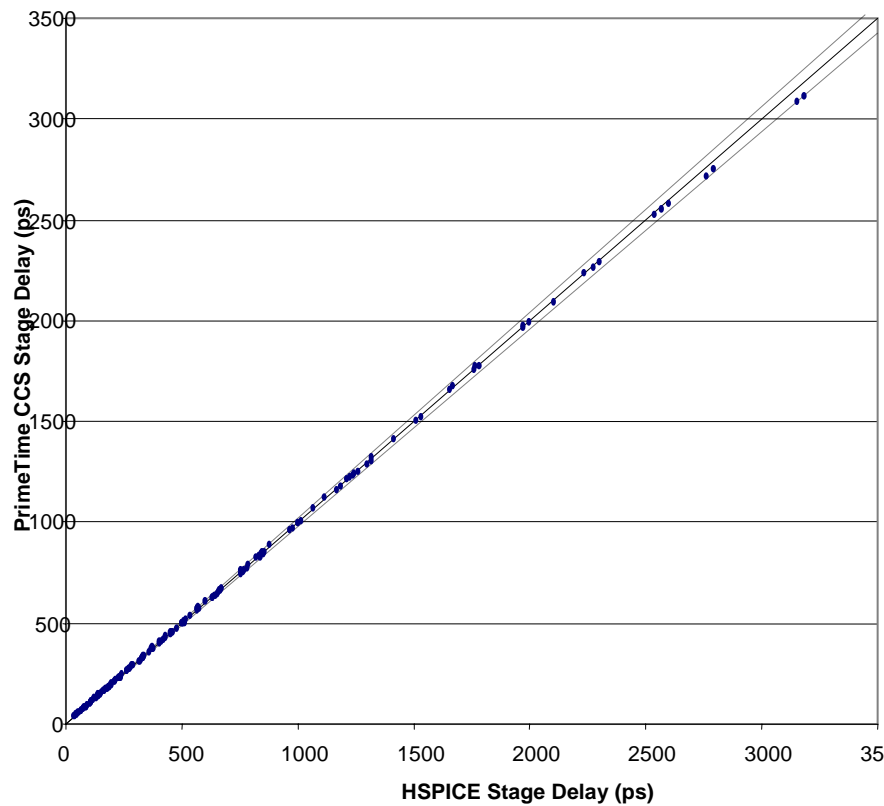
- Choose small number of $i(t)$ points so that full $v(t)$ waveform can be accurately re-created by integrating $i(t)$:

$$dv = dt * i / C_{out}$$

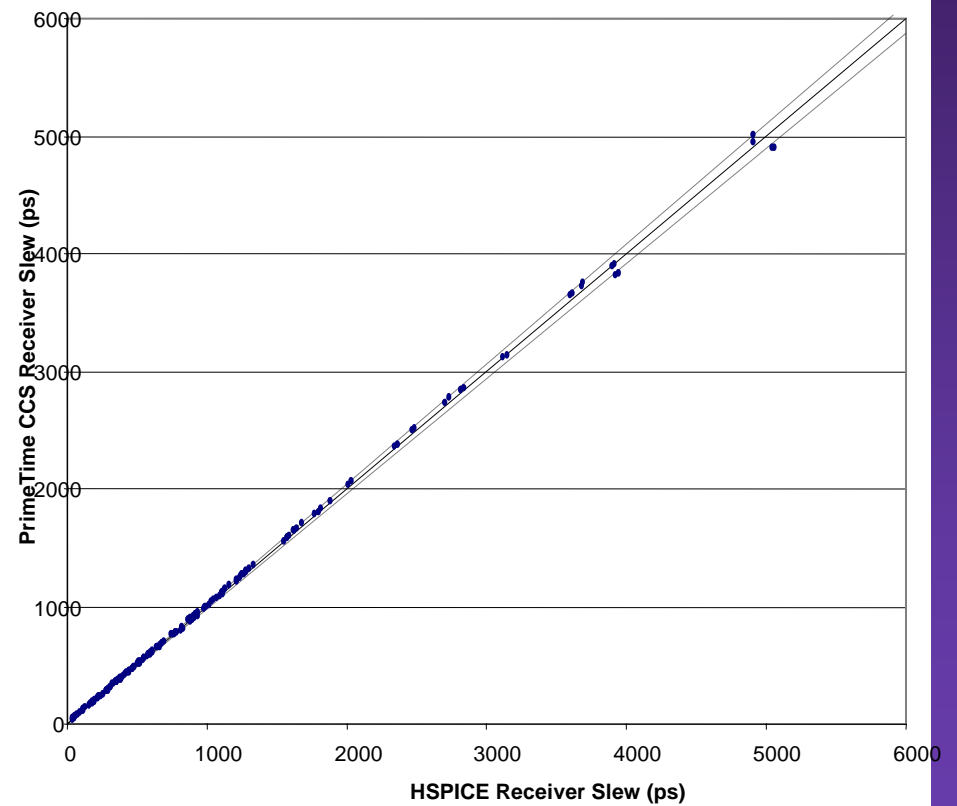
CCS Delay & Slew: 2% versus HSPICE®

Varied driver size, wire length and input slew

CCS Stage Delay vs. HSPICE



CCS Slew vs. HSPICE

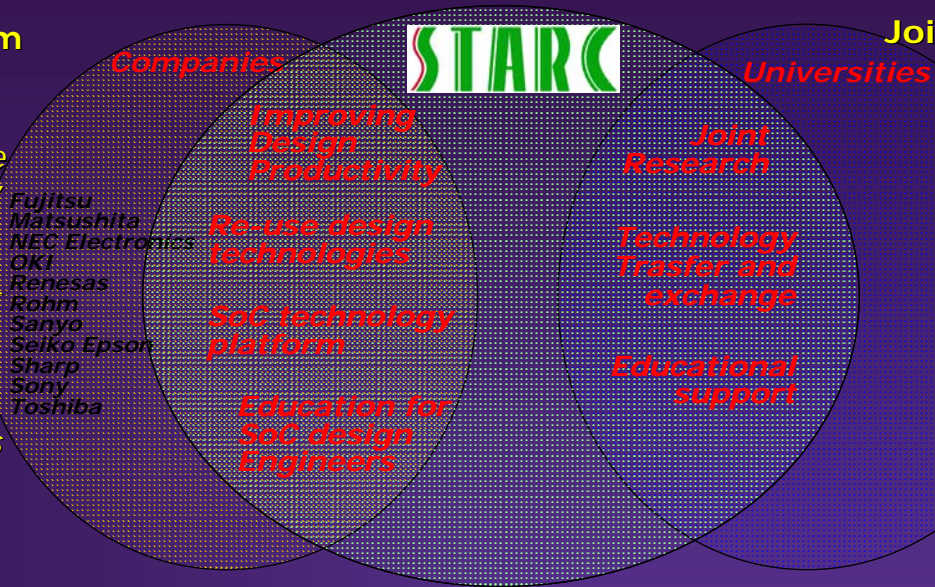




Semiconductor Technology Academic Research Center

SoC Technology Platform

- ✓ Develop standard cell libraries for SoC design
- ✓ Endeavor to revitalize the SoC business in Japan by developing an SoC technology platform
- ✓ Increase the efficiency of SoC development by promoting the popularization of standardized cell libraries and IP cores
- ✓ Increase number of SoC architects and design engineers



Joint Research with Universities

- ✓ Contract research to – and conduct joint research with – Japanese universities
- ✓ Build a effective relationship between industry and universities in the field of fundamental silicon semiconductor technologies
- ✓ Support the development of young researchers with strong interest

Value up the design platform in System LSI as industry standard

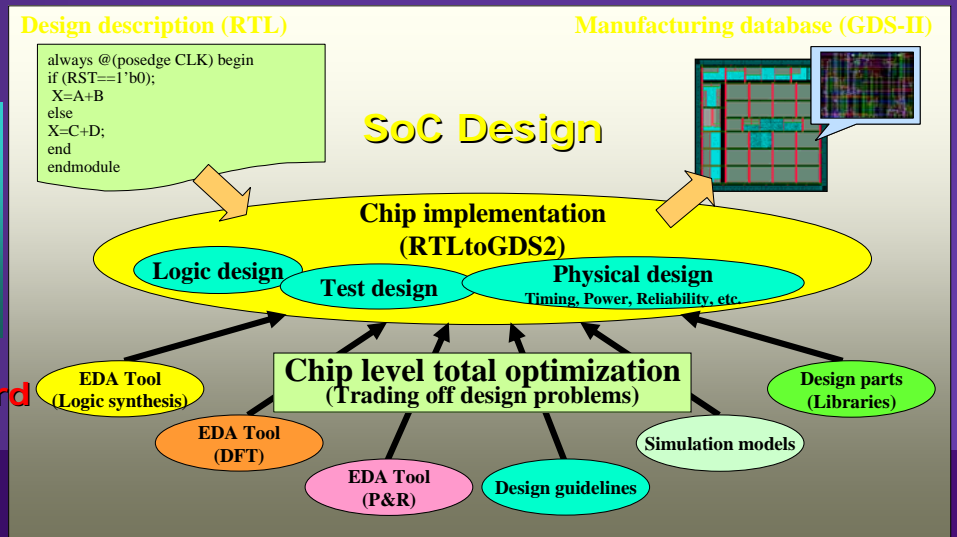
Marketing and new products



- ✓ Difficulties in design due to nanometer technology
- ✓ Huge development cost for design system

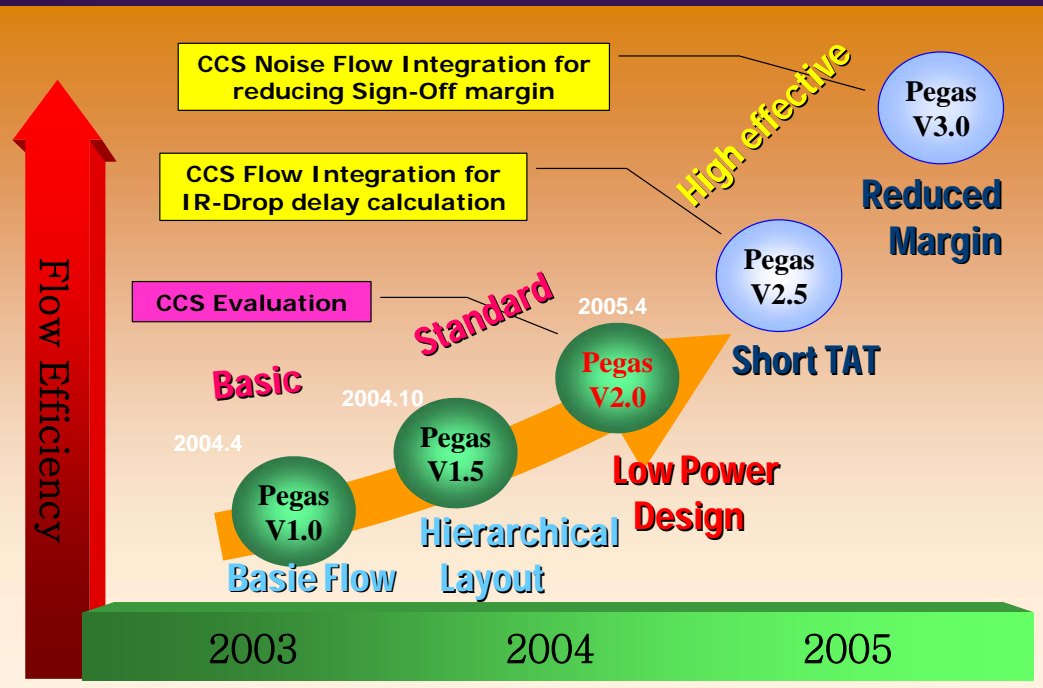
STARCAD-21™

Production flow with chip level optimization





High Efficiency Design Flow by CCS introduction



Pegas Flow : Synopsys Galaxy Platform V1.0 (2004/04)

Basic Design Flow for 90nm technology
Check & Go for Timing, SI and DFM

V1.5 (2004/10)

Hierarchical Design Flow
Multi Vth Cell Design

V2.0 (2005/04)

Low Power Design Flow (MultiVdd, Isolator)
Gated Clock and Dynamic Power Optimization

V2.5 (2005/10)

Reducing design turn around time drastically
CCS Flow Integration for IR-Drop Delay Calculation

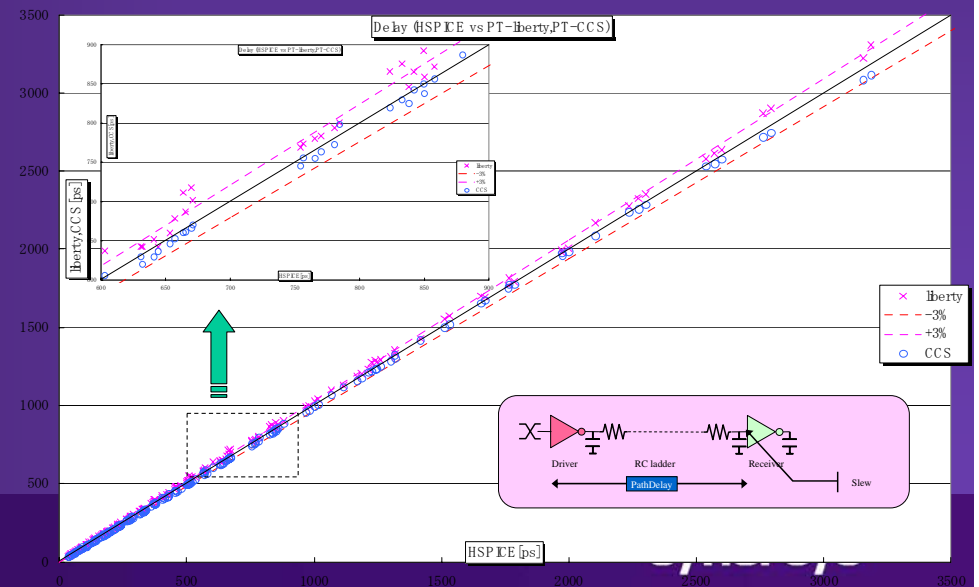
V3.0 (2006/01)

Less Design Margin by CCS Noise
Optimization of Hand-off and sign-off criteria

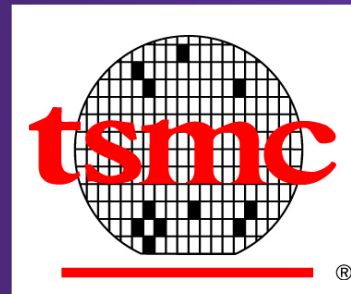
Pegas V2.0 Development

- ✓ CCS Evaluation for delay accuracy and Voltage Interpolation

PrimeTime2004.12 with STARC 90nm CCS liberty libraries
Accuracy : Very good
(< 3% against HSpice)



Industry-wide Support for CCS



Summary

- **High accuracy delay and slew calculation**
 - Advanced driver and receiver modeling
 - Results within 2% of SPICE
 - Powerful scaling for IR drop and more
- **Extensible current source technology**
 - Noise, Power, Variation
- **Tool Support**
 - 2005.06: PrimeTime[®] SI, Library Compiler[™], NanoChar
 - 2005.09: Physical Compiler[®] & Astro[™]
 - 2005.12: Galaxy[™] IC Compiler
- **Industry Support**
 - ARM, TSMC, Virage Logic, Library Technologies